A Novel Technique for 3-D Integration: Ge-seeded Laterally Crystallized TFTs

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Abstract

With increasing chip size and complexity, interconnect delays are becoming limiting factors in increasing performance. 3-D device integration will result in a reduction in chip size and interconnect delay. We present a novel technique for achieving high-performance MOS devices for vertical integration.

Poly-Ge is used as a seeding agent to laterally crystallize amorphous Si films into the channel of poly-TFTs, resulting in a substantial performance improvement through a simple, CMOS-compatible process. The technology is scaleable, and should enable near-single crystal performance in deep sub-micron devices.

Introduction

As chip complexity and size has increased, interconnect delays have become a bottleneck limiting further improvement in chip speed. The delays associated with long interconnect lines is approaching the delays associated with individual active elements within the chip. Therefore, the need exists for a means to reduce chip size and average interconnect length through vertical integration of active devices. Unfortunately, no viable techniques exist today which allow this integration to be achieved. Techniques such as SIMOX allow SOI devices to be built on a single layer, but cannot be extended for 3-D integration.

Controlled seeding in amorphous Si and subsequent lateral crystallization is a promising technique for achieving vertical integration. Crystallization occurs through nucleation and subsequent grain growth. Seeding is used to enhance nucleation in specific regions. These regions thus nucleate first and act as starting points for the lateral growth of large single-crystal islands. This controlled grain growth is the key to obtaining single-grain electronic devices. Metal-induced crystallization has been previously described (1). Unfortunately, metallic seeding agents such as Ni, are not CMOS-compatible, and therefore have questionable applicability to 3-D integration. We present a novel seeding technique which is low thermal budget, low-cost, simple, and CMOS-compatible, and is therefore extremely promising for achieving 3-D integration. Germanium is used as a seeding agent to laterally crystallize amorphous Si films. This results in large-grain polysilicon having spatially-specified grains. It is therefore possible to fabricate high-performance TFTs with excellent control over the position of grain boundaries.

We present results detailing the performance of TFTs fabricated using this technique. We discuss the extension of

this technique to deep sub-micron MOS devices for 3-D integration, offering near-single crystal performance.

Seeding and Crystallization Methodology

Ge is an excellent seeding agent for the solid-phase crystallization of amorphous Si. It can be deposited by LPCVD, and can be deposited selectively using an oxide mask over the amorphous silicon film. Poly-Ge can be deposited at low temperatures ($<400^\circ$). After Ge deposition, the Si film is crystallized at low temperature to inhibit nucleation within the film. Grains grow laterally from the seeding points due to the lower activation energy associated with the Ge-Si interface. By placing the seeding points in the source/drain regions of a TFT, it is possible to laterally crystallize into the channel. After crystallization, the Ge is removed using a standard $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$ clean. Thus the seeding technique is fully CMOS-compatible. The crystallization is a low temperature process. The thermal budget involved can be tailored to meet the needs of individual applications and device dimensions.

Device Fabrication

Devices were fabricated on oxidized silicon wafers to test the potential for 3-D integration. 100nm amorphous Si was deposited by LPCVD at 500°C followed by 50nm sacrificial SiO_2 . Seeding holes were patterned in the SiO_2 and Ge was deposited by LPCVD at 450°C using a GeH_4 chemistry. The Ge deposited selectively on the exposed Si through the holes.

Following the Ge deposition, the films were crystallized at 500°C . After crystallization, the Ge and SiO_2 were stripped using $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$ and HF respectively. Planar top-gate TFTs were then fabricated, positioning the seeding points in the source/drain regions of the devices. 30nm thermally-grown SiO_2 (grown at 1000°C) was used as a gate dielectric. For comparison, unseeded TFTs were also fabricated using an identical process. The seeding and fabrication process is shown in figure 1.

Figure 1: Process flow

Results

Electrical measurements performed on the TFTs show that the seeding technique results in a substantial improvement in performance over unseeded devices. For comparison, transfer characteristics for unseeded and seeded PMOS devices are shown in fig. 2, showing improvement in both mobility and sub-threshold performance.

Figure 2: PMOS characteristics ($W/L=0.9\mu\text{m}/0.7\mu\text{m}$)

An analysis of the effect of seeding vs. device size is used to estimate the extent of lateral crystallization. This is done for NMOS devices in figure 3. Clearly, the performance increases greatly for small devices. PMOS devices show similar trends. The device parameters are summarized below, in table I:

Figure 3: Variation in mobility with channel length.

Table I: Summary of Device Characteristics ($W/L=0.9\mu\text{m}/0.7\mu\text{m}$)				
Parameter	PMOS		NMOS	
	Ctrl	Seed	Ctrl	Seed
Field-effect mobility ($\text{cm}^2/\text{V-s}$)	70	101	100	254
Sub-threshold slope (V/dec.)	0.25	0.22	0.22	0.22
Leakage Current (pA)	1	1	5	7

Discussion

The high mobility of the seeded devices at short channel lengths suggests that Ge seeding may be an extremely useful technique for fabricating vertically integrated short-channel MOS devices. As the channel length is reduced, the laterally crystallized region becomes a larger fraction of the channel, and near-single crystal performance should result at deep sub-micron dimensions, when single-grain devices result from the scaling. The technique can be used to fabricate larger devices by optimizing the deposited amorphous Si film to maximize incubation time. The defect density within the film can also be reduced by this technique. The Si films used in this experiment were deposited by LPCVD using a silane (SiH_4) chemistry. A further performance improvement can be achieved by using disilane (Si_2H_6), which will increase the incubation time, increasing the extent of lateral crystallization and reducing the number of defects within the crystallized film (2).

The mechanism of germanium seeding is currently under study. It may occur through two processes - the actual transfer of the crystalline lattice of the poly-Ge at the Si-Ge interface, and the formation of a low incubation time SiGe alloy which crystallizes quickly and then grows laterally. Depending on the mechanism, the seeding size and location can also be optimized to further improve performance.

The simplicity and low thermal budget of this technique makes it extremely promising for 3-D integration processes. Its CMOS compatibility will result in no deleterious effects to the performance of devices on the chip. The low thermal budget of the process should enable vertical integration with minimal diffusion in underlying layers. Optimization should enable the fabrication of MOS devices having near single-crystal performance. The performance of these devices, combined with the reduction in chip area and interconnect length, should push the performance of complex VLSI circuits even further.

Conclusions

Germanium seeding has been used to form laterally crystallized polysilicon TFTs. These offer a substantial performance improvement over conventional TFTs. Mobilities of 250 (NMOS) and 100 (PMOS) have been achieved. Use of this technique should enable the fabrication of near-single crystal high-performance TFTs using a simple CMOS-compatible process, allowing the use of this technique to achieve 3-D integration for complex VLSI applications.

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References

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