2012 IEEE Silicon Nanoelectronics Workshop

Hilton Hawaiian Village

Honolulu, HI USA

June 10-11, 2012

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2012 IEEE Silicon Nanoelectronics Workshop

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Welcome Message

The 2012 IEEE Silicon Nanoelectronics Workshop is a satellite workshop of the 2012 VLSI Symposia sponsored by the IEEE Electron Device Society. It is the seventeenth workshop in the annual series, which showcases original work on nanometer-scale devices and technologies that utilize silicon or which are based on silicon substrates. The program this year includes 8 invited talks, 27 oral presentations, and 47 poster papers contributed by researchers from around the world. The Program Chair, Thomas Skotnicki, and I would like to thank the members of the Technical Program Committee and all of the attendees for their contributions and participation to make this workshop a success. We hope that you enjoy the workshop and the wonderful venue in Honolulu, Hawaii!

Tsu-Jae King Liu

General Chair, 2012 Silicon Nanoelectronics Workshop

Committee Members for the 2012 IEEE Silicon Nanoelectronics Workshop

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Tsu-Jae King Liu, *University of California at Berkeley*

Program Chair

Thomas Skotnicki, *STMicroelectronics*

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2012 IEEE Silicon Nanoelectronics Workshop

Hilton Hawaiian Village, Honolulu, HI USA
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Technical Program

Opening Remarks

Sunday, June 10, 8:30
Tsu-Jae King Liu, *University of California at Berkeley*, General Chair

Session 1: Plenary & Towards Zero Power Electronics

Sunday, June 10, 8:40
Co-chairs: Toshiro Hiramoto, *University of Tokyo* and Thomas Skotnicki, *STMicroelectronics*

8:40 **1-1** (Plenary Invited) **Innovative thermal energy harvesting for zero power electronics**, S. Monfray[1], O. Puscasu[1,2], G. Savelli[2], U. Soupremanien[2], E. Ollier[2], C. Guerin[2], L.G. Fréchette[3], E. Léveille[3], G. Mirshekari[3], C. Maitre[1], P. Coronel[2], K. Domanski[4] , P. Grabiec[4], P. Ancey[1], D. Guyomar[5], V. Bottarel[6], G. Ricotti[6], F. Boeuf[1], F. Gaillard[2], and T. Skotnicki[1], [1]*STMicroelectronics, France* [2]*CEA Liten, France* [3]*Université de Sherbrooke, Canada* [4]*ITE, Poland,* [5]*INSA Lyon, France,* [6]*STMicroelectronics, Italy*

9:10 **1-2** (Plenary Invited) **New type steep-S device using the bipolar action**, D. Hisamoto, S. Saito, A. Shima, H. Yoshimoto, and K. Torii, *Hitachi, Ltd., Japan*

9:40 **1-3** **Experimental Demonstration of Temperature Stability of Si-Tunnel FET over Si-MOSFET**, S. Migita, K. Fukuda, Y. Morita, and H. Ota, *AIST, Japan*

09:55 **1-4** **Scale laws for enhanced power for MEMS based heat energy harvesting**, O. Puscasu[1,2], S. Monfray[1], F. Boeuf[1], G. Savelli[3], F. Gaillard[3], D. Guyomar[2], T. Skotnicki[1], [1]*STMicroelectronics*, [2]*INSA Lyon*, [3]*CEA Liten, France*

Session 2: Thermal Management & Nanoscale Memory

Sunday, June 10, 10:30
Co-chairs: Byung-Gook Park, *Seoul National University* and Tsu-Jae King Liu, *UC Berkeley*

10:30 **2-1** (Invited) **Energy-Efficiency and Thermal Management in Nanoscale Devices**, *A.D. Liao, Z.-Y. Ong, A.Y. Serov, F. Xiong, and Eric Pop*, *University of Illinois at Urbana-Champaign, USA*

11:00 **2-2** **Comparative Study of Tri-Gate- and Double-Gate-Type Poly-Si Fin-Channel Split-Gate Flash Memories**, Y.X. Liu[1], T. Kamei[2], T. Matsukawa[1], K. Endo[1], S. O'uchi[1], J. Tsukada[1], H. Yamauchi[1], Y. Ishikawa[1], T. Hayashida[2], K. Sakamoto[1], A. Ogura[2], and M. Masahara[1,2], [1]*AIST* [2]*Meiji University, Japan*

11:15 **2-3** **Variation-Aware Study of BJT-based Capacitorless DRAM Cell Scaling Limit**, M.H. Cho, W. Kwon, N. Xu, and T.-J.K. Liu, *University of California at Berkeley, USA*

11:30 **2-4** **Investigation into the Effect of the Variation of Gate Dimensions on Program Characteristics in 3D NAND Flash Array**, J.Y. Seo, Y. Kim, S.H. Park, W. Kim, D.-B. Kim, J.-H. Lee, H. Shin, and B.-G. Park, *Seoul National University, Korea*

11:45 **2-5** **A novel Gate-All-Around Ultra-Thin p-channel Poly-Si TFT Functioning as Transistor and Flash Memory with Silicon Nanocrystals**, H.-B. Chen[1], S.-H. Lin[2], J.-J. Wu[1], Y.-C. Wu[2], and C.-Y. Chang[1], [1]*National Chiao Tung University* [2]*National Tsing Hua University, Taiwan ROC*

Session 3: Advanced Channel and Gate Stack Materials

Sunday, June 10, 13:30

Co-chairs: Kristin De Meyer, *IMEC* and Dong-Won Kim, *Samsung Electronics*

13:30 **3-1** (Invited) **Graphene for More Moore and More Than Moore Applications,** M.C. Lemme, S. Vaziri, A.D. Smith, J. Li, S. Rodriguez, A. Rusu, M. Ostling*, KTH Royal Institute of Technology, Sweden*

14:00 **3-2** **High Performance Ω-Gate Ge FinFET Featuring Low Temperature Si_2H_6 Passivation and Implantless Schottky-Barrier NiGe Metallic Source/Drain**, B. Liu[1], X. Gong[1], G. Han[1], P.S.Y. Lim[1], Y. Tong[1], Y. Yang[1], N. Daval[2], M. Pulido[2], D. Delprat[2], B.-Y. Nguyen[2], and Y.-C. Yeo[1], [1]*National University of Singapore, Singapore* [2]*Soitec, France*

14:15 **3-3** **High-performance pMOSFETs with High-k Gate Dielectric and Dislocation-free Epitaxial Si/Ge Super-lattice Channel**, L.-J. Liu[1], K.-S. Chang-Liao[1], C.-H. Fu[1], H.-C. Hsieh[1], C.-C. Lu[1], T.-K. Wang[1], P. Y. Gu[2], and M.J. Tsai[2], [1]*National Tsing Hua University*, [2]*Industrial Technology Research Institute, Taiwan ROC*

14:30 **3-4** **Counter Dipole Layer Formation in SiO_2/High-k/SiO_2/Si Gate Stacks**, S. Hibino, T. Nishimura, K. Nagashio, K. Kita, and A. Toriumi, *University of Tokyo, Japan*

14:45 **3-5** **Simultaneous Carrier Transport Enhancement and Variability Reduction in Si MOSFETs by Insertion of Partial Monolayers of Oxygen**, R.J. Mears[1], N. Xu[2], N. Damrongplasit[2], H. Takeuchi[1], R.J. Stephenson[1], N.W. Cody[1], A. Yiptong[1], X. Huang[1], M. Hytha[1], and T.-J.K. Liu[2], [1]*Mears Technologies* [2]*University of California at Berkeley, USA*

15:00 **3-6** **Transport in Graphene on Boron Nitride**, D.K. Ferry, *Arizona State University, USA*

Session 4: Spintronic Devices

Sunday, June 10, 15:35
Chair: Stephen Goodnick, *Arizona State University*

15:35 **4-1** (Invited) **Magnetic Tunnel Junction for Magnetoresistive Random Access Memory and Beyond,** H. Ohno, *Tohoku Univeristy, Japan*

16:05 **4-2** **Systolic Architectures and Applications for Nanomagnet Logic**, M. Niemier[1], X. Ju[2], M. Becherer[2], G. Csaba[1], X.S. Hu[1], D. Schmitt-Landsiedel[2], P. Lugli[2], and W. Porod[1], [1]*University of Notre Dame, USA* [2]*Technical University of Munich, Germany*

16:20 **4-3** **Analysis of static noise margin and power-gating efficiency of a new nonvolatile SRAM cell using pseudo-spin-MOSFETs**, Y. Shuto, S. Yamamoto, and S. Sugahara, *Tokyo Institute of Technology, Japan*

Poster Session 1: Advanced Memory and Channel Materials

Sunday, June 10, 16:40 – 19:00
Chair: Yee-Chia Yeo, *National University of Singapore*

16:40 **Poster introductions** (1 minute each)

Session 5: Emerging Memory Devices

Monday, June 11, 8:30
Co-chairs: Simon Deleonibus, *LETI* and Malgorzata Jurczak, *IMEC*

8:30 **5-1** (Invited) **Recent Progress of Resistive Switching Random Access Memory (RRAM)**, Y. Wu, S. Yu, X. Guan, and H.-S.P. Wong, *Stanford University, USA*

9:00 **5-2** **Bidirectional Selection Device Characteristics of Ultra-Thin (<3nm) TiO_2 layer for 3D Vertically Stackable ReRAM Application**, J. Woo[1], J. Park[2], J. Shin[2], G. Choi[1], S. Kim[2], W. Lee[2], S. Park[2], D. Lee[1], E. Cha[2], and H. Hwang[1], Pohang [1]*University of Science and Technology* [2]*Gwangju Institute of Science and Technology, Republic of Korea*

9:15 **5-3** **Co-existed Unipolar and Bipolar Resistive Switching Effect of HfOx-Based RRAM**, B. Chen, B. Gao, Y.H. Fu, R. Liu, L. Ma, P. Huang, F.F. Zhang, L.F. Liu, X.Y. Liu, J.F. Kang, and G.J. Lian, *Peking University, China*

9:30 **5-4** **4kb nonvolatile nanogap memory (NGpM) with 1 ns programming capability**, T. Takahashi[1], S. Furuta[1], Y. Masuda[1], S. Kumaragurubaran[1], T. Sumiya[1], M. Ono[1], Y. Hayashi[2], T. Shimizu[3], H. Suga[3], M. Horikawa[3], and Y. Naitoh[3], [1]*Funai Electric Advanced Applied Technology Research Institute* [2]*Tsukuba Device Solution Center* [3]*AIST, Japan*

9:45 **5-5** **Characteristics of Metal/Ferroelectric (PVDF-TrFE)/Graphene (MFG) Device**, H.J. Hwang, E.J. Paek, J.H. Yang, C.G. Kang, and B.H. Lee, *Gwangju Institute of Science and Technology, Korea*

Session 6: Single Electron Devices & Quantum Transport

Monday, June 11, 10:20

Co-chairs: Michiharu Tabe, *Shizuoka University* and Wolfgang Porod, *Notre Dame University*

10:20 **6-1** (Invited) **Silicon Single-Electron Transfer Devices: Ultimate Control of Electric Charge,** A. Fujiwara, G. Yamahata, K. Nishiguchi, G.P. Lansbergen, and Y. Ono, *NTT Corporation, Japan*

10:50 **6-2** **Reinvestigation of Dot Formation Mechanisms in Silicon Nanowire Channel Single-Electron/Hole Transistors Operating at Room Temperature**, R. Suzuki, M. Nozue, T. Saraya, and T. Hiramoto, *University of Tokyo, Japan*

11:05 **6-3** **Quantum Transport Property in FETs with Deterministically Implanted Single-Arsenic Ions Using Single-ion Implantation**, M. Hori[1], T. Shinada[1], F. Guagliardo[2], G. Ferrari[2], and E. Prati[3], [1]*Waseda University, Japan* [2]*Politecnico di Milano,* [3]*CNR-IMM, Italy*

11:20 **6-4** **High-frequency properties of Si single-electron transistor**, H. Takenaka[1], M. Shinohara[1], T. Uchida[1], M. Arita[1], A. Fujiwara[2], Y. Ono[2], K. Nishiguchi[2], H. Inokawa[3], and Y. Takahashi[1], [1]*Hokkaido University* [2]*NTT Corporation* [3]*Shizuoka University, Japan*

11:35 **6-5** **Negative Differential Resistance Devices with Ultra-High Peak-to-Valley Current Ratio Based on Silicon Nanowire Structure**, S. Shin, M.W. Ryu, and K.R. Kim, *Ulsan National Institute of Science and Technology, Korea*

11:50 **6-6** **Mapping of single donors in nano-scale MOSFETs at low temperature**, J. Verduijn[1,2], G.C. Tettamanzi[1], R. Wacquez[3], B. Roche[3], B. Voisin[3], X. Jehl[3], M. Sanquer[3], S. Rogge[1,2], [1]*University of New South Wales, Australia* [2]*Delft University of Technology, The Netherlands* [3]*CEA-LETI, France*

Session 7: Nanoscale Phenomena

Monday, June 11, 13:30

Co-chairs: Kazuhiko Endo, *AIST* and Yukinori Ono, *University of Toyama*

13:30 **7-1** (Invited) **A Single Atom Transistor**, M.Y. Simmons, *University of New South Wales, Australia*

14:00 **7-2** **Statistical Variability Study of a 10nm Gate Length SOI FinFET Device**, B. Cheng[1], A.R. Brown[2], X. Wang[1], and A. Asenov[1,2], [1]*University of Glasgow* [2]*Gold Standard Simulations, United Kingdom*

14:15 **7-3** **Reduced Drain Current Variability in Fully Depleted Silicon-on-Thin-BOX (SOTB) MOSFETs**, T. Mizutani[1], Y. Yamamoto[2], H. Makiyama[2], T. Tsunomura[2], T. Iwamatsu[2], H. Oda[2], N. Sugii[2], and T. Hiramoto[1], [1]*University of Tokyo* [2]*Low-power Electronics Association & Project, Japan*

14:30 **7-4** **The Impact of the Carrier Transport on the Random Dopant Induced Drain Current Variation in the Saturation Regime of Advanced Strained-Silicon CMOS Devices**, E.R. Hsieh[1], S.S. Chung[1], C.H. Tsai[2], R.M. Huang[2], C.T. Tsai[2], and C.W. Liang[2], [1]*National Chiao Tung University* [2]*United Microelectronics Corporation, Taiwan ROC*

14:45 **7-5** **On the Statistical Trap-Response (STR) Method for Characterizing Random Trap Occupancy and NBTI Fluctuation**, J. Zou[1], C. Liu[1], R. Wang[1], X. Xu[1], J. Liu[2], H. Wu[2], Y. Wang[1], R. Huang[1], [1]*Peking University* [2]*Semiconductor Manufacturing International Corporation, China*

15:00 **7-6** **Statistical distribution of RTS amplitudes in 20nm SOI FinFETs**, X. Wang[1], A.R. Brown[2], B. Cheng[1], and A. Asenov[1,2], [1]*University of Glasgow* [2]*Gold Standard Simulations, United Kingdom*

Poster Session 2: Nanoscale/Quantum Devices and Phenomena

Monday, June 11, 15:20 – 17:30
Chair: Thomas Skotnicki, *STMicroelectronics*

15:20 **Poster introductions** (1 minute each)

Poster Session 1: Advanced Memory and Channel Materials

Sunday, June 10, 16:40 – 19:00

P1-1 **Self-Improvement of Cell Stability in SRAM by Post Fabrication Technique**, A. Kumar, T. Saraya, S. Miyano, and T. Hiramoto, *University of Tokyo, Japan*

P1-2 **Improving the Endurance of Floating Gate NAND Flash Cells with Junction-Free Structure**, I. Joo[1,2], S. Hur[1], C. Lee[1], S. Lee[1], H. Park[1], J. Song[1], H. Lee[1], Y. Jun[1], and I. Chung[2], [1]*Samsung Electronics* [2]*SungKyunKwan University, Korea*

P1-3 **Low Standby Power Charge Trap Flash Memory with Tunneling Field Effect Transistor**, M.S. Han[1], J.H. Lee[2], D. Seo[1], C.-D. Park[1], Y. Oh[1], and I.H. Cho[1], [1]*Myongji University,* [2]*Seoul National University, Korea*

P1-4 **Charge-trap flash memory devices fabricated with nano-scale patterns on the Si_3H_4 trapping layer**, H.-M. An[1], K.H. Kim[1], H.-D. Kim[1], W.-J. Cho[2], and T.G. Kim[1], [1]*Korea University,* [2]*Kwangwoon University, Korea*

P1-5 **Simulation of Charge Trapping Memory with Silicon Nanocrystals Embedded in Silicon Nitride Layer**, Y. Peng, X. Liu, G. Du, Y. Yang, and J. Kang, *Peking University, China*

P1-6 **Nanodot-type Floating Gate Memory with High-density Nanodot Array Formed Utilizing *Listeria* Dps**, H. Kamitake[1], K. Ohara[1], M. Uenuma[1], B. Zheng[1], Y. Ishikawa[1], I. Yamashita[1.2], and Y. Uraoka[1], [1]*Nara Institute of Science and Technology* [2] *Panasonic Corporation, Japan*

P1-7 **Impacts of Silicon Nanocrystal Incorporation on the Transfer Characteristics of Poly-Silicon nanowire SONOS Devices**, K.-H. Lee, H.-C. Lin, and T.-Y. Huang, *National Chiao Tung University, Taiwan ROC*

P1-8 **3-D Stacked NAND Flash Memory Having Lateral Bit-Line Layers and Vertical Gate**, J.-W. Lee, M.-K. Jeong, B.-G. Park, H. Shin and J.-H. Lee, *Seoul National University, Korea*

P1-9 **Effect of Cu Insertion Layer between Top Electrode and Switching Layer on Resistive Switching Characteristics**, S. Jung, J.-H. Oh, K.-C. Ryoo, S. Kim, J.-H. Lee, H. Shin, and B.-G. Park, *Seoul National University, Korea*

P1-10 **Self-compliance Unipolar Resistive Switching and Mechanism of Cu/SiO_2/TiN RRAM Devices**, D. Yu, L.F. Liu, P. Huang, F.F. Zhang, B. Chen, B. Gao, Y. Hou, D.D. Han, Y. Wang, J.F. Kang, and X. Zhang, *Peking University, China*

P1-11 **Stable Resistive Switching Characteristics Observed in SiN-based Resistive Switching Memory Devices by using RF-sputtering methods**, H.-D. Kim, S.M. Hong, H.-M. An, K.H. Kim, Y. Seo, M. Song, D. Li, and T.G. Kim, *Korea University, Korea*

P1-12 **Rectifying Characteristics and Implementation of n-Si/HfO_2 based Devices for 1D1R-based Cross-Bar Memory Array**, F. F. Zhang, P. Huang, B. Chen, D. Yu, Y.H. Fu, L. Ma, B. Gao, L.F. Liu, X.Y. Liu, and J.F. Kang, *Peking University, China*

P1-13 **Oxygen-induced High-*k* Degradation in TiN/HfSiO Gate Stacks**, T. Hosoi, Y. Odake, K. Chikaraishi, H. Arimura, N. Kitano, T. Shimura, and H. Watanabe *, Osaka University, Japan*

P1-14 **Metal/Ge Schottky Barrier Modulation With C-Containing Layer by Chemical Bath**, W. Wang, J. Wang, M. Zhao, R. Liang, and J. Xu*, Tsinghua University, China*

P1-15 **Orientation and Size Effects on Ballistic Electron Transport Properties in Gate-All-Around Rectangular Germanium Nanowire FETs**, S. Mori, N. Morioka, J. Suda, and T. Kimoto*, Kyoto University, Japan*

P1-16 **Quantum Transport Simulation of III-V MOSFETs based on Wigner Monte Carlo Approach**, Y. Maegawa, S. Koba, H. Tsuchiya, and M. Ogawa*, Kobe University, Japan*

P1-17 **Mechanisms of Ambient Dependent Mobility Degradation in the Graphene MOSFETs on SiO_2 Substrate**, Y.G. Lee, C.G. Kang, C. Cho, Y.H. Kim, H.J. Hwang, J.J. Kim, U.J. Jung, E. J. Park, M.W. Kim, and B.H. Lee*, Gwangju Institute of Science and Technology, Korea*

P1-18 **Electronic Band Structures of Graphene Nanomeshes**, R. Sako, N. Hasegawa, H. Tsuchiya, and M. Ogawa*, Kobe University, Japan*

P1-19 **Band Structure and Electron Transport in Multi-Junction Graphene Nanoribbons**, N. Hasegawa, R. Sako, H. Tsuchiya, and M. Ogawa, *Kobe University, Japan*

P1-20 **Graphene-Diamond-Silicon Devices with Increased Current-Carrying Capacity: sp^2-Carbon-sp^3-Carbon-on-Silicon Technology**, J. Yu[1], G. Liu[1], A.V. Sumant[2], and A. A. Balandin[1], [1]*University of California at Riverside,* [1]*Argonne National Laboratory, USA*

P1-21 ***Selective* Gas Sensing with a *Single* Graphene-on-Silicon Transistor**, A.A. Balandin[1], S. Rumyantsev[2], G. Liu[1], M.S. Shur[2], and R.A. Potyrailo[3], [1]*University of California at Riverside* [2]*Rensselaer Polytechnic Institute,* [3]*GE Global Research, USA*

P1-22 **Graphene Fillers for Ultra-Efficient Thermal Interface Materials**, K.M.F. Shahil, V. Goyal, R. Gulotty, and A.A. Balandin, *University of California at Riverside, USA*

P1-23 **Silicon Microfabrication Technologies for THz applications**, C. Jung-Kubiak, J. Gill, T. Reck, C. Lee , J. Siles, G. Chattopadhyay, R. Lin, K. Cooper and I. Mehdi, *Jet Propulsion Laboratory, California of Technology*

Poster Session 2: Nanoscale/Quantum Devices and Phenomena

Monday, June 11, 15:20 – 17:30

P2-1 **Simulation Study on Process Conditions for High-Speed Silicon Photodetector and Quantum-Well Structuring for Increased Number of Wavelength Discriminations**, S. Cho[1], H. Kim[2], M.-C. Sun[2], T.I. Kamins[1], B.-G. Park[2], and J.S. Harris, Jr.[1], *Stanford University, USA* [2]*Seoul National University, Korea*

P2-2 **Nano-Transfer Printing of Functioning MIM Tunnel Diodes**, Mario Bareiß[1], B. Weiler[1], D. Kälblein[2], U. Zschieschang[2], H. Klauk[2], G. Scarpa[1], B. Fabel[1], P. Lugli[1], and W. Porod[3], [1]*Technische Universität München, Germany* [2]*Max Planck Institute for Solid State Research, Germany* [3]*University of Notre Dame, USA*

P2-3 **Fabrication and evaluation of heavily P-doped Si quantum dot and back-gate induced Si quantum dot**, J. Kamioka[1], T. Kodera[1,2], K., Horibe[1], Y. Kawano[1], and S. Oda[1], [1]*Tokyo Institute of Technology* [3]*University of Tokyo Japan*

P2-4 **Microwave manipulation of electrons in silicon quantum dots**, T. Ferrus[1], A. Rossi[1], T. Kodera[2,3], T. Kambara[2], W. Lin[2], S. Oda[2], and D.A. Williams[1], [1]*Hitachi Cambridge Laboratory, United Kingdom* [2]*Tokyo Institute of Technology* [3]*University of Tokyo Japan*

P2-5 **Charge sensing of a Si triple quantum dot system using single electron transistors**, R. Mizokuchi, T. Kodera, K. Horibe, Y. Kawano, and S. Oda*, Tokyo Institute of Technology, Japan*

P2-6 **Fabrication and characterization of Si/SiGe quantum dots with capping gate**, T. Kodera[1,2], Y. Fukuoka[1], K. Takeda[2], T. Obata[2], K. Yoshida[2], K. Sawano[3], K. Uchida[1], Y. Shiraki[3], S. Tarucha[2], and S. Oda[1], *Tokyo Institute of Technology* [2]*University of Tokyo* [3]*Tokyo City University, Japan*

P2-7 **Single Ge quantum dot placement along with self-aligned electrodes for effective management of single electron tunneling**, I. H. Chen, K. H. Chen, and P. W. Li*, National Central University, Taiwan ROC*

P2-8 **Single-electron transport through a single donor at elevated temperatures**, E. Hamid, D. Moraru, T. Mizuno and M. Tabe*, Shizuoka University, Japan*

P2-9 **The Interplay of Self-Heating Effects and Static RTF in Nanowire Transistors**, D. Vasileska, A. Hossain, and S.M. Goodnick*, Arizona State University, USA*

P2-10 **Effect of Interfacial States on the technological variability of Trigate MOSFETs**, E. González-Marín, F.G. Ruiz, A. Godoy, I.M. Tienda-Luna, F. Gámiz*, Universidad de Granada, Spain*

P2-11 **Evolution of Channel Trap Distribution under Bias Stress in Polysilicon Thin Film Transistors evaluated by Charge Pumping Method**, C.N. Manh[1], J.S. Chang[1], T.-Y. Jang[1], M. Hasan[1], H. Yang[1], J.K. Jeong[1], B. Kim[2], J. Ahn[2], K. Hwang[2], and R. Choi[1], [1]*Inha University* [2]*Samsung Electronics Co., Ltd., Korea*

P2-12 **Physical Model for Random Telegraph Noise Amplitudes and Implications**, R.G. Southwick III[1], K.P. Cheung[1], J.P. Campbell[1], S.A. Drozdov[2], J.T. Ryan[1], J.S. Suehle[1], and A.S. Oates[3], [1]*National Institute of Standards and Technology,* [2]*University of Maryland USA* [3]*Taiwan Semiconductor Manufacturing Company Ltd., Taiwan ROC*

P2-13 **Optoelectrical Lifetime Evaluation of Single Holes in SOI MOSFET**, W. Du[1], D.S. Putranto[1,2], H. Satoh[1], A. Ono[1], P.S. Priambodo[2], D. Hartanto[2], and H. Inokawa[1] [1]*Shizuoka University, Japan* [2]*University of Indonesia, Indonesia*

P2-14 ***Ab initio*** **analysis of donor state deepening in Si nano-channels**, D. Moraru[1], Y. Kuzuya[1], E. Hamid[1], T. Mizuno[1], M. Tabe[1], and H. Mizuta[2], [1]*Shizuoka University, Japan* [2]*University of Southampton, United Kingdom*

P2-15 **Channel Length-Dependent Series Resistance?**, J.P. Campbell[1], K.P. Cheung[1], S.A. Drozdov[2], R.G. Southwick[1], J.T. Ryan[1], A.S. Oates[3], J.S. Suehle[1], [1]*National Institute of Standards and Technology,* [2]*University of Maryland USA* [3]*Taiwan Semiconductor Manufacturing Company Ltd., Taiwan ROC*

P2-16 **Effects of Amorphous Silicon Atomic Density Variation on Series and Contact Resistances in Nanoscale Thin-Film Structures**, M.W. Ryu, S.-H. Kim, and K.R. Kim, *Ulsan National Institute of Science and Technology, Korea*

P2-17 **Evaluation of Scattering in Asymmetric Quasi-Ballistic DG-MOSFET**, G. Liu, G. Du, T. Lu, X. Liu, P. Zhang, and X. Zhang, *Peking University, China*

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