BSIM-IMG102.6.0

Independent Multi-Gate MOSFET Compact Model

Technical Manual

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1 Introduction

The continuous evolution and enhancement of bulk CMOS technology has fueled the growth of the microelectronics industry over the past several decades. When we reach the end of the technology roadmap for the classical CMOS, multiple gate CMOS structures will likely take up the baton. We have developed a multiple gate MOSFET compact model for technology/circuits development in the short term and for product design in the longer term.

Several different multi-gate (MG) structures and two different modes of operation are being pursued in the industry today. In the case of planar double gate (Figure 1), the two gates will likely be asymmetric—having different work functions and dielectric thicknesses, complicating the compact model. Also, the two gates are likely to be biased at two different voltages, and these gates are called independent gates. In the other double, triple, or all-around gate cases, the gates are biased at the same voltage, and these cases are called common gate. One example of a common gate device is the FinFET transistor.

![Planar double-gate SOI MOSFET](image)

Figure 1: Planar double-gate SOI MOSFET.

The Independent Multi-Gate model BSIM-IMG described in this document has been developed to model the electrical characteristics of the independent double-gate structures. It allows different front- and back- gate work functions, dielectric thicknesses and dielectric constants.

A separate model, BSIM-CMG, has been developed to model the common-gate MG structure. Code and documentation for BSIM-CMG are also available upon request.

2 Model Description

The BSIM-IMG 102.6.0 models the independent double-gate structure as a four terminal device, containing the source(s), drain(d), front gate(fg), and back gate(bg) terminals. The two gates (e.g., 1=fg, 2=bg) are allowed to have different workfunctions ($\Delta \psi_1$, $\Delta \psi_2$) and dielectric thicknesses ($T_{ox1}, T_{ox2}$). They can also be biased separately at different voltages.

Physical surface-potential-based formulations are derived in both intrinsic and extrinsic models of BSIM-IMG. Surface potentials and integrated charge densities at the source and drain ends are obtained by solving the Poisson’s equation in a fully-depleted, lightly-doped body and calculating with efficient analytical approximations. Since the surface potential equation is derived based on Poisson’s equation,
the model captures volume inversion effects very well and shows excellent scalability compared with 2D device simulation.

To meet the requirements of future devices, new parameters has been included to model devices consisting of novel materials. This includes parameters for non-silicon channel devices and High-K gate insulators.

The back gate of a planar double-gate SOI FET is often used for tuning device threshold voltage ($V_{th}$). Therefore, the effect of back-gate on $V_{th}$ must also be addressed by the model. The threshold voltage of FDSOI transistor is extracted from constant current method as shown in Figure 2. When the back gate bias ($V_{bg}$) is low, the threshold voltage follow a linear relationship. For higher back-gate bias, however, the back-gate effect slows down as a result of back surface accumulation.

The strength of back-gate control is often quantified as $\gamma$, defined as:

$$
\gamma = \frac{dV_{th}}{dV_{bg}}
$$

When the gate length is long, $\gamma$ can be approximated using

$$
\gamma = \frac{dV_{th}}{dV_{bg}} \approx -\frac{C_{ox2} \parallel C_{si}}{C_{ox1}}
$$

where $C_{ox1} = \epsilon_{ox1}/T_{ox1}$, $C_{ox2} = \epsilon_{ox2}/T_{ox2}$, $C_{si} = \epsilon_{si}/T_{si}$. This long channel $\gamma$ is inherently captured by the core model of BSIM-IMG. There are two inversion charge density models for the body charge available in the core of the model, which can be selected using the parameter CHARGEMOD. CHARGEMOD=0 is a simplified and computationally efficient charge density model which is the default model used in the core. A more accurate but computationally intensive charge density model, appropriate for body thickness less than 2 nm, can be selected using CHARGEMOD=1. As we shrink the gate length,
Figure 3: $\gamma$ versus gate length. Symbols: TCAD; Lines: Model

Figure 4: $V_{th}$ roll-off for different back-gate biases. Symbols: TCAD; Lines: Model
\( \gamma \) is reduced due to the capacitive coupling from the source/drain (Figure 3). In BSIM-IMG, the length dependence of \( \gamma \) is model by equation (3.107), (3.109). Using a length-dependent \( \gamma \), the model successfully captures \( V_{th} \) roll-off for different back-gate biases, as shown in Figure 4.

Other important effects, such as short channel effects, mobility degradation, velocity saturation, velocity overshoot, series resistance, channel length modulation, quantum mechanical effects, gate tunneling current, gate-induced-drain-leakage, and parasitic capacitance, are also incorporated in the model.

The model continuous and is symmetric at \( V_{ds}=0 \). This physics-based model is scalable and predictive over a wide range of device parameters.

## 3 BSIM-IMG 102.6.0 Model Equations

### 3.1 Bias Independent Calculations

#### 3.1.1 Physical Constants

Physical quantities in BSIM-IMG are in M.K.S units unless specified otherwise.

\[
q = 1.6 \times 10^{-19} \quad (3.3)
\]
\[
\epsilon_0 = 8.8542 \times 10^{-12} \quad (3.4)
\]
\[
k = 1.3787 \times 10^{-23} \quad (3.5)
\]
\[
\epsilon_{si} = EPSRSUB \cdot \epsilon_0 \quad (3.6)
\]
\[
\epsilon_{sub} = EPSRSUB \cdot \epsilon_0 \quad (3.7)
\]
\[
\epsilon_{ox1} = EPSROX1 \cdot \epsilon_0 \quad (3.8)
\]
\[
\epsilon_{ox2} = EPSROX2 \cdot \epsilon_0 \quad (3.9)
\]
\[
\epsilon_{ratio} = \frac{EPSRSUB}{3.9} \quad (3.10)
\]
\[
C_{ox1} = \frac{3.9 \cdot \epsilon_0}{EOT1} \quad (3.11)
\]
\[
C_{ox2} = \frac{3.9 \cdot \epsilon_0}{EOT2} \quad (3.12)
\]
\[
C_{ox1P} = \frac{3.9 \cdot \epsilon_0}{EOT1P} \quad (3.13)
\]
\[
C_{ox2P} = \frac{3.9 \cdot \epsilon_0}{EOT2P} \quad (3.14)
\]
\[
C_{si} = \frac{\epsilon_{si}}{TSI} \quad (3.15)
\]
\[
\nu_{tm} = \frac{kT}{q} \quad (3.16)
\]
\[
\delta_2 = 10^{-3} \quad (3.17)
\]
3.1.2 Effective Channel Length and Channel Width

\[ L_{\text{new}} = L + XL \]  
\[ L_{\text{LLN}} = L_{\text{new}} - L_{\text{LLN}} \]  
\[ L_{\text{WLN}} = L_{\text{new}} - L_{\text{WLN}} \]  
\[ LW_{\text{LLN-LWN}} = L_{\text{LLN}} \cdot W_{\text{WLN}} \]  
\[ d\text{LIV} = L\text{INT} + LL \cdot L_{\text{LLN}} + LW \cdot W_{\text{WLN}} + LWL \cdot LW_{\text{LLN-LWN}} \]  
\[ L_{\text{eff}} = L_{\text{new}} - 2.0 \cdot d\text{LIV} \]  

Here, \( d\text{LIV} \) is the overlap/underlap between the gate and the source/drain diffusions; \( L\text{INT} \) is \( d\text{LIV} \) for large devices; \( L \) is the designed (drawn) length; \( XL \) is the length variation due to process effects; \( LL, LW, LWL \) and \( L_{\text{LLN}}, W_{\text{WLN}}, LW_{\text{LLN-LWN}} \) are fitting parameters.

\[ d\text{LCV} = DLC + LLC \cdot L_{\text{LLN}} + LWC \cdot W_{\text{WLN}} + LWLC \cdot LW_{\text{LLN-LWN}} \]  
\[ L_{\text{effCV}} = L_{\text{new}} - 2.0 \cdot d\text{LCV} \]  

Here, \( d\text{LCV} \) is the overlap/underlap between the gate and the source/drain diffusions for C-V calculations; \( DLC \) is \( d\text{LCV} \) for large devices; \( LLC, LWC, LWLC \) and \( L_{\text{LLN}}, W_{\text{WLN}}, LW_{\text{LLN-LWN}} \) are fitting parameters. \( \text{NFMOD} \) switch is used for \( W_{\text{new}} \) calculation, when \( \text{NFMOD} \) is 0: \( W \) is taken as total width like BSIM4 and when \( \text{NFMOD} \) is 1: \( W \) is taken as single finger width.

\[ W_{\text{new}} = \begin{cases} W_{\text{NF}} & \text{NFMOD}=0 \\ W_{\text{NFMOD}} & \text{NFMOD}=1 \end{cases} \]  
\[ W_{\text{new}} = W + XW \]  
\[ W_{\text{WLN}} = W_{\text{new}} - LW_{\text{WLN}} \]  
\[ W_{\text{WWN}} = W_{\text{new}} - WW_{\text{WWN}} \]  
\[ LW_{\text{WLN-WWN}} = L_{\text{WLN}} \cdot W_{\text{WWN}} \]  
\[ d\text{WIV} = W\text{INT} + WL \cdot L_{\text{WLN}} + WW \cdot W_{\text{WWN}} + WWL \cdot LW_{\text{WLN-WWN}} \]  
\[ W_{\text{eff}} = W_{\text{new}} - 2.0 \cdot d\text{WIV} \]  

Here, \( d\text{WIV} \) is gate edge adjacent to STI for I-V calculations; \( W\text{INT} \) is \( d\text{WIV} \) for large devices; \( W \) is the designed (drawn) length; \( XW \) is the length variation due to process effects; \( WL, WW, WWL \) and \( L_{\text{WLN}}, W_{\text{WWN}}, LW_{\text{WLN-WWN}} \) are fitting parameters.

\[ d\text{WCV} = DWC + WLC \cdot L_{\text{WLN}} + WWC \cdot W_{\text{WWN}} + WWLC \cdot LW_{\text{WLN-WWN}} \]  
\[ W_{\text{effCV}} = W_{\text{new}} - 2.0 \cdot d\text{WCV} \]  

Here, \( d\text{WCV} \) is gate edge adjacent to STI for C-V calculations; \( DWC \) is \( d\text{WCV} \) for large devices; \( WLC, WWC, WWLC \) and \( L_{\text{WLN}}, W_{\text{WWN}}, LW_{\text{WLN-WWN}} \) are fitting parameters.

3.1.3 Binning Calculations

The optional binning methodology [1] is adopted in BSIM-IMG. In the binning methodology, the device \( W, L \) is divided into many bins according to the required model accuracy. For a given geometry, each model parameter
$\text{PARAM}_i$ is calculated as a function of a zero-order term, $\text{PARAM}$, a length dependent term, L$\text{PARAM}$, a width dependent term, W$\text{PARAM}$, and a WL product dependent term, P$\text{PARAM}$:

$$\text{PARAM}_i = \text{PARAM} + \frac{1}{L_{\text{eff}}} \cdot \text{L} \text{PARAM} + \frac{1}{W_{\text{eff}}} \cdot \text{W} \text{PARAM} + \frac{1}{W_{\text{eff}}L_{\text{eff}}} \cdot \text{P} \text{PARAM}$$ \hspace{1cm} (3.34)

For the list of binnable parameters, please refer to the complete parameter list in the end of this technical note.

### 3.1.4 Length scaling equations

$$U_0[L] = \begin{cases} U_{0i} \cdot [1 - U_{Pi} \cdot L_{\text{eff}}^{-LPA}] & \text{LPA} > 0 \\ U_{0i} \cdot [1 - U_{Pi}] & \text{Otherwise} \end{cases}$$ \hspace{1cm} (3.35)

$$M\text{EXP}[L] = M\text{EXP}_i + A\text{MEXP} \cdot L_{\text{eff}}^{-M\text{EXP}}$$ \hspace{1cm} (3.36)

$$P\text{CLM}[L] = P\text{CLM}_i + A\text{PCLM} \cdot \exp \left( -\frac{L_{\text{eff}}}{B\text{PCLM}} \right)$$ \hspace{1cm} (3.37)

$$U\text{A}[L] = U\text{A}_i + A\text{UA} \cdot \exp \left( -\frac{L_{\text{eff}}}{B\text{UA}} \right)$$ \hspace{1cm} (3.38)

$$E\text{U}[L] = E\text{U}_i + A\text{EU} \cdot \exp \left( -\frac{L_{\text{eff}}}{B\text{EU}} \right)$$ \hspace{1cm} (3.39)

$$U\text{D}[L] = U\text{D}_i + A\text{UD} \cdot \exp \left( -\frac{L_{\text{eff}}}{B\text{UD}} \right)$$ \hspace{1cm} (3.40)

$$U\text{DB}[L] = U\text{DB}_i + A\text{UDB} \cdot \exp \left( -\frac{L_{\text{eff}}}{B\text{UDB}} \right)$$ \hspace{1cm} (3.41)

$$U\text{C}[L] = U\text{C}_i + A\text{UC} \cdot \exp \left( -\frac{L_{\text{eff}}}{B\text{UC}} \right)$$ \hspace{1cm} (3.42)

$$P\text{TWG}[L] = P\text{TWG}_i + A\text{PTWG} \cdot \exp \left( -\frac{L_{\text{eff}}}{B\text{PTWG}} \right)$$ \hspace{1cm} (3.43)

$$P\text{TWGB}[L] = P\text{TWGB}_i + A\text{PTWGB} \cdot \exp \left( -\frac{L_{\text{eff}}}{B\text{PTWGB}} \right)$$ \hspace{1cm} (3.44)

$$P\text{TWGR}[L] = P\text{TWGR}_i + A\text{PTWG} \cdot \exp \left( -\frac{L_{\text{eff}}}{B\text{PTWG}} \right)$$ \hspace{1cm} (3.45)

$$V\text{SAT}[L] = V\text{SAT}_i + A\text{VSAT} \cdot \exp \left( -\frac{L_{\text{eff}}}{B\text{VSAT}} \right)$$ \hspace{1cm} (3.46)

$$V\text{SATB}[L] = V\text{SATB}_i + A\text{VSATB} \cdot \exp \left( -\frac{L_{\text{eff}}}{B\text{VSATB}} \right)$$ \hspace{1cm} (3.47)

$$V\text{SAT1}[L] = V\text{SAT1}_i + A\text{VSAT1} \cdot \exp \left( -\frac{L_{\text{eff}}}{B\text{VSAT1}} \right)$$ \hspace{1cm} (3.48)

$$V\text{SATCV}[L] = V\text{SAT}_i + A\text{VSATCV} \cdot \exp \left( -\frac{L_{\text{eff}}}{B\text{VSATCV}} \right)$$ \hspace{1cm} (3.49)

$$V\text{SAT1}[L] = V\text{SAT1}_i + A\text{VSAT1} \cdot \exp \left( -\frac{L_{\text{eff}}}{B\text{VSAT1}} \right)$$ \hspace{1cm} (3.50)
If \( RDSMOD = 0 \) then
\[
RDSW[L] = RDSW_i + ARDSW \cdot \exp \left( - \frac{L_{eff}}{BRDSW} \right)
\]
(3.51)

If \( RDSMOD = 1 \) then
\[
RSW[L] = RSW_i + ARSW \cdot \exp \left( - \frac{L_{eff}}{BRSW} \right)
\]
(3.52)
\[
RDW[L] = RDW_i + ARDW \cdot \exp \left( - \frac{L_{eff}}{BRDW} \right)
\]
(3.53)

3.1.5 Temperature Effects

\[
E_g = BG0SUB - \frac{TBGASUB \cdot T^2}{T + TBGBSUB}
\]
(3.54)
\[
n_i = NI0SUB \cdot \left( \frac{T}{300.15} \right)^{\frac{3}{2}} \cdot \exp \left( \frac{BG0SUB \cdot q}{2k \cdot 300.15} - \frac{E_g \cdot q}{2k \cdot T} \right)
\]
(3.55)
\[
N_c = NC0SUB \cdot \left( \frac{T}{300.15} \right)^{\frac{3}{2}}
\]
(3.56)
\[
V_{bi} = \frac{kT}{q} \cdot \ln \left( \frac{NSD \cdot NBODY}{n_i^2} \right)
\]
(3.57)
\[
\Phi_B = \frac{kT}{q} \cdot \ln \left( \frac{NBODY}{n_i} \right)
\]
(3.58)
\[
\Phi_{SUB} = \frac{kT}{q} \cdot \ln \left( \frac{NBG}{n_i} \right)
\]
(3.59)
\[
\Delta V_{th, temp} = \left( KT1 + \frac{KT1L}{L_{eff}} \right) \cdot \left( \frac{T}{TNOM} - 1 \right) + \left( KT2 + \frac{KT2L}{L_{eff}} \right) \cdot \left( \frac{T}{TNOM} - 1 \right) \cdot V_{bgx}
\]
(3.60)
\[
\mu_0(T) = U0[L] \cdot \left( \frac{T}{TNOM} \right)^{UTE_i} + UTL_i \cdot (T - TNOM)
\]
(3.61)
\[
MEXP(T) = MEXP[L] \cdot (1.0 + TMEXP \cdot (T - TNOM))
\]
(3.62)
\[
ETAMOB(T) = ETAMOB_i \cdot [1 + EMOBT_i \cdot (T - TNOM)]
\]
(3.63)
\[
UA(T) = UA[L] + UA1_i \cdot (T - TNOM)
\]
(3.64)
\[
UC(T) = UC[L] + UC1 \cdot (T - TNOM)
\]
(3.65)
\[
UD(T) = UD[L] \cdot \left( \frac{T}{TNOM} \right)^{UD1_i}
\]
(3.66)
\[
UCS(T) = UCS_i \cdot \left( \frac{T}{TNOM} \right)^{UCSTE_i}
\]
(3.67)
\[ ETA_0(T) = ETA_0[L] \cdot (1.0 + TETA_0 \cdot (T - TNOM)) \quad (3.68) \]

\[ AT = AT \cdot (1.0 + \frac{10^{-6}}{L_{eff}} \cdot ATL) \quad (3.69) \]

\[ ATB = ATB \cdot (1.0 + \frac{10^{-6}}{L_{eff}} \cdot ATBL) \quad (3.70) \]

\[ VSAT(T) = VSAT[L] \cdot (1 - AT \cdot (T - TNOM)) \quad (3.71) \]

\[ VSAT1(T) = VSAT1[L] \cdot (1 - AT \cdot (T - TNOM)) \quad (3.72) \]

\[ VSATB(T) = VSATB[L] \cdot (1 - ATB \cdot (T - TNOM)) \quad (3.73) \]

\[ VSATCV(T) = VSATCV[L] \cdot (1 - AT \cdot (T - TNOM)) \quad (3.74) \]

\[ PTWG(T) = PTWG[L] \cdot (1 - PTWGT \cdot (T - TNOM)) \quad (3.75) \]

\[ BETA_0(T) = BETA_0[i] \cdot \left( \frac{T}{TNOM} \right)^{HT} \quad (3.76) \]

\[ K_0(T) = K_0[i] + K01[i] \cdot (T - TNOM) \quad (3.77) \]

\[ K0SI(T) = K0SI[i] + K0SI1[i] \cdot (T - TNOM) \quad (3.78) \]

\[ BGIDL(T) = BGIDL[i] \cdot (1 + TGIDL \cdot (T - TNOM)) \quad (3.79) \]

\[ BGISL(T) = BGISL[i] \cdot (1 + TGISL \cdot (T - TNOM)) \quad (3.80) \]

\[ RDSWMIN(T) = RDSWMIN \cdot (1 + PRT \cdot (T - TNOM)) \quad (3.81) \]

\[ RDSW(T) = RDSW[L] \cdot (1 + PRT \cdot (T - TNOM)) \quad (3.82) \]

\[ RSWMIN(T) = RSWMIN \cdot (1 + PRT \cdot (T - TNOM)) \quad (3.83) \]

\[ RDWMIN(T) = RDWMIN \cdot (1 + PRT \cdot (T - TNOM)) \quad (3.84) \]

\[ RSW(T) = RSW[L] \cdot (1 + PRT \cdot (T - TNOM)) \quad (3.85) \]

\[ RDW(T) = RDW[L] \cdot (1 + PRT \cdot (T - TNOM)) \quad (3.86) \]

\[ R_{s,geo}(T) = R_{s,geo} \cdot (1 + PRT \cdot (T - TNOM)) \quad (3.87) \]

\[ R_{d,geo}(T) = R_{d,geo} \cdot (1 + PRT \cdot (T - TNOM)) \quad (3.88) \]

\[ Igtemp = \left( \frac{T}{TNOM} \right)^{IGT} \quad (3.89) \]

### 3.1.6 Front and Back Gate Workfunction Calculation

\[ PHIG2_i = \begin{cases} PHIG2 + 0.5 \cdot BG0SUB - \Phi_{SUB} & \text{for N-WELL} \\ PHIG2 - 0.5 \cdot BG0SUB + \Phi_{SUB} & \text{for P-WELL} \end{cases} \quad (3.90) \]
\[ \Phi_{\text{ref}} = \begin{cases} \text{EASUB} & \text{for NMOS} \\ \text{EASUB} + E_g & \text{for PMOS} \end{cases} \] (3.91)

\[ \text{devsign} = \begin{cases} 1 & \text{for NMOS} \\ -1 & \text{for PMOS} \end{cases} \] (3.92)

\[ \Delta \Phi_1 = \text{devsign} \cdot (PHIG_1 - \Phi_{\text{ref}}) \] (3.93)

\[ \Delta \Phi_2 = \text{devsign} \cdot (PHIG_2 - \Phi_{\text{ref}}) \] (3.94)

\[ \Phi_{sd} = \text{EASUB} + \frac{E_g}{2} - \text{devsign} \cdot \min \left[ \frac{E_g}{2}, \frac{kT}{q} \cdot \ln \left( \frac{\text{NSD}}{n_i} \right) \right] \] (3.95)

\[ V_{fbsd} = \text{devsign} \cdot (PHIG_1 - \Phi_{sd}) \] (3.96)

### 3.2 Terminal Voltages and Pre-conditioning

#### 3.2.1 Terminal Voltages and \( V_{dsx} \) Calculation

\[ V_{fgs} = V_f - V_s \] (3.97)

\[ V_{fgd} = V_f - V_d \] (3.98)

\[ V_{bgs} = V_b - V_s \] (3.99)

\[ V_{bgd} = V_b - V_d \] (3.100)

\[ V_{ds} = V_d - V_s \] (3.101)

\[ V_{gfb1} = V_{fgs} - \Delta \Phi_1 \] (3.102)

\[ V_{gfb2} = V_{bgs} - \Delta \Phi_2 \] (3.103)

\[ V_{dsx} = \sqrt{V_{ds}^2 + 0.0004} - 0.02 \] (3.104)

\[ \text{symmetry factor} = \frac{1}{2} (V_{dsx} - V_{ds}) \] (3.105)

\[ V_{bgx} = V_{bgs} + \text{symmetry factor} \] (3.106)
3.2.2 Back Gate Biasing Effect

If p-well

\[ K_{vb} = KBG0PW - \frac{0.5 \cdot KBG1PW}{\cosh(DBGPW \cdot \frac{L_{eff}}{\lambda})} \]  \hspace{1cm} (3.107)

\[ K_{vb}^{*} = KBG2PW + \frac{1}{2} \left[ K_{vb} - KBG2PW + \sqrt{(K_{vb} - KBG2PW)^2 + 0.0001} \right] \]  \hspace{1cm} (3.108)

If n-well

\[ K_{vb} = KBG0NW - \frac{0.5 \cdot KBG1NW}{\cosh(DBGNW \cdot \frac{L_{eff}}{\lambda})} \]  \hspace{1cm} (3.109)

\[ K_{vb}^{*} = KBG2NW + \frac{1}{2} \left[ K_{vb} - KBG2NW + \sqrt{(K_{vb} - KBG2NW)^2 + 0.0001} \right] \]  \hspace{1cm} (3.110)

\[ \gamma_0 = -\frac{C_{ox2} \cdot C_{si}}{(C_{ox2} + C_{si}) \cdot C_{ox1}} \]  \hspace{1cm} (3.111)

\[ V_{gfb\text{eff}} = V_{gfb2n} - symmetry \text{ factor} \]  \hspace{1cm} (3.112)

where, \( V_{gfb2n} \) is the clamp limit for the back-gate bias (\( V_{gfb2n} = -1.2 \)). \( \lambda \) is characteristic length and defined in equation 3.131.

3.2.3 Back-gate Depletion

Parameter BPFACTORPW (BPFACCTORNW for N-type back gate) is used to invoke the effect of backplane doping in the model (i.e., BPFACTORPW (BPFACCTORNW) \( \neq 0 \) to invoke the back gate depletion effect) and VKNee1PW (VKNee1NW) is used to set the back-gate voltage at which measured data starts deviating from straight line behavior.
If P-type back gate

\[ \text{welsign} = -1 \]  
\[ V_{\text{knee}1} = VKNEE1PW \]  
\[ V_{\text{knee}2} = VKNEE2PW \]  
\[ \text{bpfactor} = BPFACCTORPW \]  

If N-type back gate

\[ \text{welsign} = 1 \]  
\[ V_{\text{knee}1} = VKNEE1NW \]  
\[ V_{\text{knee}2} = VKNEE2NW \]  
\[ \text{bpfactor} = BPFACCTORNW \]  

3.2.4 Calculation of Threshold Voltage Shift due to Back Gate Depletion Effect

\[ T_0 = \begin{cases} \sqrt{1 + \frac{\max [\text{welsign} (V_{bgx} - V_{\text{knee}1})_0]}{V_{\text{subdep}0}}} - 1 & \text{NMOS} \\ \sqrt{1 + \frac{\max [-\text{welsign} (V_{bgx} + V_{\text{knee}1})_0]}{V_{\text{subdep}0}}} - 1 & \text{PMOS} \end{cases} \]  

\[ V_{\text{subdep}0} = \frac{1}{2} \frac{q \cdot NBE_{\text{sub}}}{C^2_{ox}} \]  

\[ V_{\text{subdep}} = V_{\text{subdep}0} \cdot T_0^2 \]  

\[ T_1 = -V_{\text{subdep}0} + V_{\text{knee}2} - 10^{-2} \]  

\[ V_{\text{subdep}} = -V_{\text{knee}2} + \frac{1}{2} \left[ T_1 + \sqrt{T_1^2 + 0.04 \cdot V_{\text{subdep}0}} \right] \]  

\[ \Delta V_{\text{th,vbg}} = \begin{cases} \gamma_0 \cdot K_{vbg} \cdot [V_{gfb2} - (\text{welsign} \cdot \text{bpfactor} \cdot V_{\text{subdep}}) - V_{gfb2e,ff}] & \text{NMOS} \\ \gamma_0 \cdot K_{vbg} \cdot [V_{gfb2} + (\text{welsign} \cdot \text{bpfactor} \cdot V_{\text{subdep}}) - V_{gfb2e,ff}] & \text{PMOS} \end{cases} \]
3.3 Short Channel Effects

3.3.1 Scale Length $\lambda$

\[
\lambda_f = \sqrt{TSI \cdot \epsilon_{ratio} \cdot EOT1}
\]
\[
\lambda_s = \sqrt{TSI \cdot \left(\epsilon_{ratio} \cdot EOT1 + \frac{3}{8} \cdot TSI\right)}
\]
\[
T_0 = \frac{V_{gfb1} \cdot EOT2 \cdot \epsilon_{ratio} + V_{gfb2} \cdot (EOT1 \cdot \epsilon_{ratio} + TSI)}{t_{eff}} + \text{symmetry factor}
\]
\[
x_\lambda = \frac{1}{2} + \frac{1}{\pi} \tan^{-1} [ASCL + BSCL \cdot T_0]
\]
\[
\lambda = \lambda_s + x_\lambda (\lambda_f - \lambda_s)
\]

3.3.2 $V_t$ Roll-off

\[
\phi_{st} = 0.4 + \Phi_B + PHIN_i
\]
\[
\Delta V_{th,SCE} = -0.5 \cdot \frac{DVT_0}{\cosh \left(DVT_1 \cdot \frac{L_{eff}}{\lambda}\right) - 1} \cdot (V_{bi} - \phi_{st})
\]

3.3.3 Drain Induced Barrier Lowering (DIBL)

\[
\Delta V_{th,DIBL} = - \frac{0.5 \cdot (ETA0(T) + ETAB[L] \cdot V_{bgx})}{\cosh \left(DSUB \cdot \frac{L_{eff}}{\lambda}\right) - 1} \cdot V_{dsx}
\]

3.3.4 $V_t$ Roll on/off at moderate channel lengths

\[
\Delta V_{th,RSC} = K1RSCE \cdot \left[\sqrt{1 + \frac{LPE0}{L_{eff}}} - 1\right] \cdot \sqrt{\phi_{st}}
\]

3.3.5 $V_t$ Roll on/off at moderate channel lengths and high $V_{ds}$

\[
\Delta V_{th,DSC} = - \frac{DSC0}{DSC1 + L_{eff}} \cdot V_{dsx}
\]
3.3.6 Sub-threshold Slope Degradation

\[ V_{bgxpos} = 0.5 \cdot \left( V_{bgx} + \sqrt{V_{bgx}^2 + 4 \cdot \delta_2^2} \right) \]  (3.137)

\[ \delta_1 = (CDSCD + CBGCBGD \cdot V_{bgxpos}) \cdot V_{dsx} \]  (3.138)

\[ \theta_{SCE} = \frac{0.5}{\cosh\left(DVT1 \cdot \frac{I_{off}}{A}\right)} - 1 \]  (3.139)

\[ C_{dsc} = CBGCBG0 \cdot V_{bgx} + CBGCBG0P \cdot V_{bgx}^2 \]  (3.140)

\[ + \theta_{SCE} \cdot (CDSC + CBGCBG \cdot V_{bgx} + CBGCBGP \cdot V_{bgx}^2 + \delta_1) \]

\[ n = 1 + \frac{CIT + C_{dsc}}{C_{ox1} + C_{si} \parallel C_{ox2}} \]  (3.141)

where \( \delta_2 \) is defined in equation 3.17.

3.3.7 Body Doping Effects

\[ \Delta V_{th,nbody} = \frac{q \cdot NBODY \cdot TSI}{C_{ox1}} \left[ 1 - \frac{0.5 \cdot TSI}{TSI + \epsilon_{ratio} \cdot EOT2} \right] \]  (3.142)

3.3.8 Cumulative Threshold Voltage Adder

\[ \Delta V_{th,all} = \Delta V_{th,vtral} + \Delta V_{th,dsib} + \Delta V_{th,rsce} + \Delta V_{th,dsc} + \Delta V_{th,nbody} + \Delta V_{th,temp} + \Delta V_{th,vbg} \]  (3.143)

3.4 Surface Potential Calculation

Surface Potential is computed solving the Poisson’s equation in silicon body [2]

\[ E_{S1}^2 - E_{S2}^2 = \frac{2N_{DOS}kT}{\epsilon_{Si}} \left( e^{\frac{\psi_{s1} - V_{ch}}{\epsilon_{Si} / t_{eff}}} - e^{\frac{\psi_{s2} - V_{ch}}{\epsilon_{Si} / t_{eff}}} \right) \]  (3.144)

where \( N_{DOS} \) is the conduction band/valence band density of states for NMOS/PMOS transistor and \( V_{ch} \) is the channel potential. \( E_{S1} \), the front side electric field and \( E_{S2} \), the back side electric field are given by

\[ E_{S1} = \frac{C_{ox1}(V_{gfb1eff} - \psi_{s1})}{\epsilon_{si}} \]  (3.145)

\[ E_{S2} = \frac{C_{ox2}(V_{gfb2eff} - \psi_{s2})}{\epsilon_{si}} \]  (3.146)
where

\[ V_{gfb1eff} = V_{gfb1} - \Delta V_{th,all} \]  
\[ V_{gfb2eff} = V_{gfb2n} \]  

Equation (3.144) is simplified, similar to [3], replacing \( v_{tm} \) by \( n v_{tm} \) and neglecting the second exponential term on right side. Further approximating \( \psi_s2 \) to be

\[ \psi_s2 = \frac{C_{si}}{C_{si} + C_{ox2}} \psi_s1 + \frac{C_{ox2}}{C_{si} + C_{ox2}} V_{gfb2eff} \]  

The simplified Poisson’s equation is obtained as

\[ \left(\frac{C_{ox1} V_{gfb1eff} - \psi_s1}{\epsilon_{Si}}\right)^2 - \left(\frac{V_{gfb2eff} - \psi_s1}{TSI + \frac{\epsilon_{si}}{\epsilon_{ox}} EOT2}\right)^2 = \frac{2N_{DOS}kT}{\epsilon_{Si}} \left( e^{\psi_s1 - \nu_{ch}} \right) \]  

This is rewritten as

\[ f(x) \equiv \left(\frac{\nu_{gfb1} - x}{G}\right)^2 - B_{sq} (\nu_{gfb2} - x)^2 - e^{(x - \nu_{ch})} = 0 \]  

where

\[ \nu_{gfb1} = \frac{V_{gfb1eff}}{n v_{tm}} \]  
\[ \nu_{gfb2} = \frac{V_{gfb2eff}}{n v_{tm}} \]  
\[ \nu_{ch} = \frac{V_{ch}}{n v_{tm}} \]  
\[ x = \frac{\psi_s1}{n v_{tm}} \]  
\[ G = \frac{EOT1}{\epsilon_{ox}} \sqrt{\frac{2qN_{DOS}\epsilon_{si}}{n v_{tm}}} \]  
\[ B_{sq} = \left( \frac{1}{TSI} + \frac{\epsilon_{si}}{\epsilon_{ox}} EOT2 \sqrt{\frac{\epsilon_{si} n v_{tm}}{2qN_C}} \right)^2 \]  

The implicit equation (3.151) is solved using an iterative Halley’s algorithm for a maximum of four iterations stopping when the error in surface potential solution is below 1 nV. Halley’s algorithm is a second order Householder’s method and can be written as

\[ x_{n+1} = x_n - \frac{2f(x)f'(x)}{2[f'(x)]^2 - f(x)f''(x)} \]
where the iterant solutions $x_n$, $x_{n+1}$ are related using $f'(x)$ and $f''(x)$, the first and second derivatives of equation (3.151) with respect to $x$. The initial guess for $x$ is taken to be $\psi_{s1}/nv_{tm}$, where $\psi_{s1}$ is the solution of (3.159). Equation (3.159) is obtained simplifying (3.144), assuming back-gate to remain always in very weak inversion, reducing it to become a function of only the front-gate parameters.

$$
\left( C_{ox1} \frac{V_{gfb1e} - \psi_{s1}^0}{\epsilon_{Si}} \right)^2 = \frac{2N_{DOS}kT}{\epsilon_{Si}} \left( \frac{\psi_{s1}^0 - V_{ch}}{e^{\frac{\psi_{s1}^0 - V_{ch}}{nv_{tm}}}} \right)
$$

(3.159)

The implicit equation (3.159) is solved using two iterations of Halley’s algorithm, the solution to (3.159) is always stable and $\bar{\psi}_{s1}^0$ given by (3.160), as the initial guess [4].

$$
\bar{\psi}_{s1}^0 = \begin{cases} 
V_{gfb1e} & \text{if } V_{gfb1e} \leq 0 \\
\min \left[ V_{gfb1e}, \left( V_{ch} + 2nv_{tm} \ln \left( \frac{V_{gfb1e}C_{ox1}}{2qN_{c}nv_{tm}\epsilon_{si}} \right) \right) \right] & \text{if } V_{gfb1e} > 0
\end{cases}
$$

(3.160)

Once $x$ satisfying (3.151) is known, $\psi_{s1}$ is obtained from $x$ using (3.161) and $\psi_{s2}$ is obtained from $\psi_{s1}$ using (3.149).

$$
\psi_{s1} = x \cdot nv_{tm}
$$

(3.161)

Equation (3.151) is solved once at the source side, with $V_{ch} = 0$, and once at drain side, with $V_{ch} = V_{ds}$, to obtain the surface potentials at the two ends of the channel. More details can be found in [2]. The electric field and total inversion charges are then obtained as follows.

### 3.5 Calculation of Integrated Inversion Charge Density

As shown below, for CHARGEMOD=0 (default), the inversion charge density at source and drain ends in the body is calculated using [2].
### 3.5.1 For CHARGEMOD=0

At source end: \((V_{ch} = 0)\)

\[
\psi_{fs} = \psi_{s1} \tag{3.162}
\]

\[
\psi_{bs} = \psi_{s2} \tag{3.163}
\]

\[
E_{S1} = \frac{V_{gfb\text{eff}} - \psi_{fs}}{EOT1} \tag{3.164}
\]

\[
E_{S2} = \frac{\psi_{fs} - \psi_{bs}}{TSI} \tag{3.165}
\]

\[
T_1 = \frac{1}{2}(\psi_{fs} - \psi_{bs}) + \frac{1}{2}\sqrt{((\psi_{fs} - \psi_{bs})^2 + 0.000004 \cdot (n_{vtm})^2)} \tag{3.166}
\]

\[
Q_{\text{tots}} = \frac{2qN_{\text{DOS}}n_{vtm}}{E_{S1} + E_{S2}} \exp\left(\frac{\psi_{bs} - V_{ch}}{n_{vtm}}\right) \exp\left(\frac{T_1}{n_{vtm}} - 1\right) \tag{3.167}
\]

At drain end: \((V_{ch} = V_{ds})\)

\[
\psi_{fd} = \psi_{s1} \tag{3.168}
\]

\[
\psi_{bd} = \psi_{s2} \tag{3.169}
\]

\[
E_{S1} = \frac{V_{gfb\text{eff}} - \psi_{fd}}{EOT1} \tag{3.170}
\]

\[
E_{S2} = \frac{\psi_{fd} - \psi_{bd}}{TSI} \tag{3.171}
\]

\[
T_1 = \frac{1}{2}(\psi_{fd} - \psi_{bd}) + \frac{1}{2}\sqrt{((\psi_{fd} - \psi_{bd})^2 + 0.000004 \cdot (n_{vtm})^2)} \tag{3.172}
\]

\[
Q_{\text{totd}} = \frac{2qN_{\text{DOS}}n_{vtm}}{E_{S1} + E_{S2}} \exp\left(\frac{\psi_{bd} - V_{ch}}{n_{vtm}}\right) \exp\left(\frac{T_1}{n_{vtm}} - 1\right) \tag{3.173}
\]

For body thickness less than 2 nm, a more accurate formulation of inversion charge density is needed. [3] develops the inversion charge density model valid for any generic body thickness and CHARGEMOD=1 makes use of this model. The increase in accuracy comes at a cost of slight increase in computation time.

### 3.5.2 For CHARGEMOD=1

\[
E_1 = \frac{V_{gfb\text{eff}} - \psi_{s1}}{\epsilon_{\text{ratio}} \cdot EOT1} \tag{3.174}
\]

\[
A = \frac{2qN_{\text{DOS}}n_{vtm}}{\epsilon_{si}} \tag{3.175}
\]

\[
D = E_1^2 - A \cdot \exp\left(\frac{\psi_{s1} - V_{ch}}{n_{vtm}}\right) \tag{3.176}
\]
If $D = 0$ then
\[
T_1 = \exp \left( -\frac{\psi_{s1} - V_{ch}}{2n\nu_{tm}} \right) + \sqrt{A \cdot TSI} \frac{1}{2n\nu_{tm}}
\]
\[\mathcal{E}_2 = \frac{\sqrt{A}}{T_1}\] (3.177)

If $D < 0$ then
\[
\theta_{20} = \frac{\sqrt{-D}}{n\nu_{tm}} \cdot \frac{TSI}{2} - \cos^{-1} \left[ \frac{-D}{A} \cdot \frac{e^{-\psi_{s1} - V_{ch}}}{n\nu_{tm}} \right]
\]
\[
\theta_{20}^* = \begin{cases} \theta_{20} & \mathcal{E}_1 > 0 \\ |\theta_{20}| & \mathcal{E}_1 \leq 0 \end{cases}
\]
\[
\mathcal{E}_2 = -\sqrt{-D} \cdot \tan(\theta_{20}^*)
\] (3.180)

If $D > 0$ then
\[
C = \frac{\exp \left( -\frac{\text{sgn}(\mathcal{E}_1) \cdot \sqrt{D} \cdot TSI}{2n\nu_{tm}} \right)}{\sqrt{ \frac{D}{A} \exp \left( -\frac{\psi_{s1} - V_{ch}}{n\nu_{tm}} \right) + 1 + \sqrt{ \frac{D}{A} \exp \left( -\frac{\psi_{s1} - V_{ch}}{n\nu_{tm}} \right) } } }
\]
\[
\mathcal{E}_2 = \text{sgn}(\mathcal{E}_1) \cdot \sqrt{D} \cdot \frac{1 + C^2}{1 - C^2}
\] (3.183)

At source end: ($V_{ch} = 0$)
\[
\psi_{fs} = \psi_{s1}
\]
\[
\psi_{bs} = \psi_{s2}
\]
\[
E_{S1} = \mathcal{E}_1
\]
\[
E_{S2} = \mathcal{E}_2
\]
\[
Q_{tots} = \epsilon_{si}(\mathcal{E}_1 - \mathcal{E}_2)
\] (3.185)

At drain end: ($V_{ch} = V_{ds}$)
\[
\psi_{fd} = \psi_{s1}
\]
\[
\psi_{bd} = \psi_{s2}
\]
\[
E_{S1} = \mathcal{E}_1
\]
\[
E_{S2} = \mathcal{E}_2
\]
\[
Q_{tots} = \epsilon_{si}(\mathcal{E}_1 - \mathcal{E}_2)
\] (3.189)
### 3.6 Drain Saturation Voltage

The drain saturation voltage model is calculated after the source-side surface potential ($\psi_s$) has been calculated. $V_{dseff}$ is subsequently used to compute the drain-side surface potential ($\psi_d$).

#### 3.6.1 Electric Field Calculations

\[
\eta = \begin{cases} 
\frac{1}{2} \cdot ETAMOB & \text{for NMOS} \\
\frac{1}{3} \cdot ETAMOB & \text{for PMOS}
\end{cases}
\]

\[q_{is} = \frac{Q_{tots}}{C_{ox1}}\]  
\[q_{bs} = q \cdot NBODY \cdot TSI \frac{C_{ox1}}{C_{ox1}}\]  
\[T_2 = \eta \cdot q_{is} + q_{bs} + E_{S2} \frac{\epsilon_{si}}{C_{ox1}}\]  
\[T_3 = \frac{1}{2}(T_2 + \sqrt{T_2^2 + 0.001})\]  
\[E_{effs} = 10^{-8} \frac{C_{ox1}}{\epsilon_{si}} T_3\]

#### 3.6.2 Drain Saturation Voltage

\[D_{mobs} = 1 + (UA(T) + UC(T) \cdot V_{bgs}) \cdot (E_{effs})^{EU} + \frac{UD(T)}{\left(\frac{1}{2} \cdot \left(1 + \frac{q_{is}}{10^{-2}/C_{ox1}}\right)\right)^{UCS(T)}}\]  
\[E_{sat} = \frac{2 \cdot VSAT(T)}{\mu_0(T)D_{mobs}}\]

Note: RDSMOD is parasitic resistance mode selector switch. Details of RDSMOD is discussed in Section 3.15.

\[RDSMOD = 0\]

\[T_6 = KSATIV \cdot \left(\frac{Q_{tots}}{C_{ox1} + C_{ox2}} + 2V_t \cdot KSUBIV\right)\]

\[a = 2W \cdot VSAT \cdot C_{ox1} \cdot R_{ds}(V)\]  
\[b = T_6 + E_{sat} L_{eff} + 3T_6 W_{eff} \cdot VSAT \cdot C_{ox1} \cdot R_{ds}(V)\]  
\[c = T_6 \cdot [E_{sat} L_{eff} + T_6 \cdot a]\]  
\[V_{dsat} = \frac{b - \sqrt{b^2 - 2ac}}{a}\]
\[ RDSMOD = 1 \]
\[ V_{d_{sat}} = \frac{E_{sat}L_{eff} \left( \frac{Q_{tots}}{C_{ox1} + C_{ox2}} \right)}{E_{sat}L_{eff} + \frac{Q_{tots}}{C_{ox1} + C_{ox2}}} \]  

(3.208)

Then [5],
\[ V_{dseff} = \frac{V_{ds}}{1 + \left( \frac{V_{ds}}{V_{d_{sat}}} \right)^{\frac{1}{MEXP}}}^{MEXP} \]  

(3.209)

3.7 Average Field, Potential, and Charge Calculation

\[ q_{ia} = \frac{Q_{tots} + Q_{totd}}{2C_{ox1}} \]  

(3.210)

\[ q_{ba} = \frac{qN_A \cdot TSI}{C_{ox1}} \]  

(3.211)

\[ E_{ba} = \frac{E_{bs} + E_{bd}}{2} \]  

(3.212)

\[ \Delta \psi = \psi_{fd} - \psi_{fs} \]  

(3.213)

\[ \Delta q_i = \frac{Q_{tots} - Q_{totd}}{C_{ox1}} \]  

(3.214)

(3.215)

3.8 Quantum Mechanical Effects

Effects that arise due to electrical confinement in the ultra-thin body SOI are dealt in this section. Currently, only the C-V effect, the bias-dependence of effective oxide thickness due to the inversion charge centroid being away from the interface, is included in the model.

\[ T5 = 1 + \left( \frac{q_{ia} + ETAQM \cdot q_{ba}}{QM0} \right)^{PQM} \]  

(3.216)

\[ C_{ox,eff} = \begin{cases} 
\frac{EOT1P \frac{3.9}{3.9 - 0.1} \frac{QMTCENCV}{Q_{ratio}}}{C_{ox1P}} & \text{if } QMTCENCV > 0 \\
C_{ox1P} & \text{if } QMTCENCV \leq 0
\end{cases} \]  

(3.217)
3.9 Mobility Degradation

Effective transverse field ($E_{effm}$) gets modified by introducing the parameter CHARGEWF. This parameter changes the average charge which goes into the effective transverse field calculation (+1:source-side, 0:middle, -1:drain-side).

$$q_{ia2} = \begin{cases} 
0.5 \cdot (q_{is} + q_{id}) & \text{for CHARGEWF} = 0 \\
0.5 \cdot (q_{is} + q_{id}) + CHARGEWF \cdot (1 - \exp(-\frac{a}{2}) \cdot 0.5 \cdot \Delta q_i) & \text{for CHARGEWF} \neq 0 
\end{cases}$$

where $a$ is defined in equation 3.204. The mobility model is based on the BSIM4 model [6].

$$T_2 = \eta \cdot q_{ia2} + q_{ba} + E_{ba} \cdot \frac{\epsilon_{si}}{C_{ox1}}$$

$$T_3 = \frac{1}{2}(T_2 + \sqrt{T_2^2 + 0.001})$$

$$E_{effm} = 10^{-8} \cdot \frac{C_{ox1}}{\epsilon_{si}} \cdot T_3$$

$$D_{mob0} = 1 + (UA(T) + UC(T) \cdot V_{bgx}) \cdot (E_{effm})^{EU} + \frac{UD(T) + UDB \cdot V_{bgx}}{U_{CS(T)}}$$

$$D_{mob} = \frac{D_{mob0}}{U_{0MULT}}$$

3.10 Lateral Non-uniform Doping Model

Lateral non-uniform doping along the length of the channel leads to I-V and C-V display different threshold voltages. However, the self-consistent surface potential based I-V and C-V model doesn’t allow for the usage of different Vth values. A straightforward method would be to re-compute the surface potentials at the source and drain end twice for I-V and C-V separately breaking the consistency but at the expense of computation time. The below model has been introduced as a multiplicative factor to the drain current (I-V) to allow for that Vth shift. This model should be exercised after the C-V extraction step to match the Vth for the subthreshold region Id,lin-Vg curve. Parameter K0 is used to fit the subthreshold region, while parameter K0SI helps reclaim the fit in the inversion region.

$$M_{nud} = \exp \left( -\frac{K0(T)}{K0SI(T) \cdot q_{ia} + 2.0 \cdot \frac{nkt}{q}} \right)$$

A word of CAUTION: The above lateral non-uniform doping model is empirical and has its limits as to how much Vth shift can be achieved without distorting the I-V curve. Over usage could lead to
negative $g_m$ or negative $g_{ds}$. The lateral non-uniform doping model could be used in combination with the mobility model to achieve high Vth shift between C-V and I-V curved to avoid any distortion of higher order derivatives.

### 3.11 Output Conductance

Channel length modulation and DIBL effects are considered to model the output conductance.

#### 3.11.1 Channel Length Modulation

\[
\frac{1}{C_{clm}} = \begin{cases} 
PCLM + PCLMG \cdot q_{ia} & \text{for } PCLMG \geq 0 \\
\frac{1}{PCLM - PCLMG \cdot q_{ia}} & \text{for } PCLMG < 0
\end{cases} 
\]  

\[
M_{clm} = \begin{cases} 
1 + \frac{1}{C_{clm}} \ln \left[ 1 + \frac{V_{ds} - V_{ds_{eff}}}{V_{ds_{sat}} + P_{sat} \cdot C_{clm}} \right] & \text{for } PCLM > 0 \\
1 & \text{for } PCLM \leq 0
\end{cases}  
\]  

\[ \text{PVAGfactor} = \begin{cases} 
1 + PVAG \cdot \frac{q_{ia}}{V_{ds_{sat}} + P_{sat} \cdot C_{clm}} & \text{for } PVAG > 0 \\
1 - PVAG \cdot \frac{q_{ia}}{V_{ds_{sat}} + P_{sat} \cdot C_{clm}} & \text{for } PVAG \leq 0
\end{cases} \]  

\[
\theta_{rout} = \frac{0.5 \cdot PDIBL1}{\cosh \left( DROUT \cdot \frac{L_{eff}}{\lambda} \right)} + PDIBL2 
\]  

\[
V_{ADIBL} = \frac{q_{ia} + 2kT/q}{\theta_{rout}} \cdot \left( 1 - \frac{V_{ds_{sat}}}{V_{ds_{sat}} + q_{ia} + 2kT/q} \right) \cdot \text{PVAGfactor} 
\]  

\[
M_{oc} = \left( 1 + \frac{V_{ds} - V_{ds_{eff}}}{V_{ADIBL}} \right) \cdot M_{clm} 
\]

$M_{oc}$ is multiplied to $I_{ds}$ in the final drain current expression.

#### 3.12 Velocity Saturation

The following formulation models the current degradation factor due to velocity saturation in the linear region. It is adopted from the BSIM5 model [7, 8].
\[
E_{sat1} = \frac{2 \cdot V_{SAT1}(T)}{\mu_0(T)D_{mobs}}
\]

(3.232)

\[
\delta_{usat} = DELTAVSAT
\]

(3.233)

\[
T_0 = 0.8 + V_{SATB}(T) \cdot V_{bgx}
\]

(3.234)

\[
X_{sat} = 0.2 + \left[ \frac{T_0 + \sqrt{T_0^2 + 0.01}}{2} \right]
\]

(3.235)

\[
D_{usat} = \frac{1 + \sqrt{\delta_{usat} + \left( \frac{\Delta q_i}{E_{sat1}L_{eff} \cdot X_{sat}} \right)^2}}{1 + \sqrt{\delta_{usat}}}
\]

(3.236)

\[
+ \frac{1}{2} \cdot (PTWG(T) - PTWGB \cdot V_{bgxpos} - PTWGB2 \cdot V_{bgx}) \cdot q_{ia} \cdot \Delta q_i^2
\]

3.13 Drain Current Model

\[
i_{ds0} = q_{ia} \cdot \Delta \psi + V_1 \cdot \Delta q_i
\]

(3.237)

\[
I_{ds0} = \mu_0 \cdot C_{ox1} \cdot \frac{W_{eff}}{L_{eff}} \cdot i_{ds0} \cdot \frac{M_{oc}}{D_{mob} \cdot D_r \cdot D_{vsat}}
\]

(3.238)

\[
I_{ds} = I_{ds0} \cdot NF
\]

(3.239)

See section 3.15 for the definition of series resistance term Dr.

3.14 C-V Model

3.14.1 C-V Model (Front Surface)

\[
T_0 = \frac{C_{ox2}}{C_{ox1}} \cdot \frac{C_{si}}{C_{ox2} + C_{si}}
\]

(3.240)

\[
T_1 = \frac{1 + T_0}{2}
\]

(3.241)

\[
T_2 = V_{gb1eff} + T_0 \cdot V_{gb2eff} + \nu_t \cdot \left( 1 + \frac{C_{ox2}}{C_{ox1}} \right)
\]

(3.242)

\[
T_3 = \psi_{fs} + \psi_{fd}
\]

(3.243)

\[
T_4 = \psi_{fd} - \psi_{fs}
\]

(3.244)

\[
T_5 = V_{gb1eff} - \frac{T_3}{2}
\]

(3.245)

\[
T_6 = \frac{T_1 \cdot T_4}{6(T_2 - T_1 T_3)}
\]

(3.246)

\[
q_{fg} = T_5 + T_6 T_4 + \Delta V_{th,vbg}
\]

(3.247)

\[
q_{11} = \frac{T_5}{2} + \frac{T_6 T_4}{10} - \frac{T_6/T_1}{10(T_2 - T_1 T_3)} (5T_2 - 4T_1 \psi_{fd} - 6T_1 \psi_{fs}) \cdot (T_2 - 2T_1 \psi_{fd})
\]

(3.248)
3.14.2 C-V Model (Back Surface)

\[ T_0 = \frac{C_{ox1}}{C_{ox2}} \cdot \frac{C_{si}}{C_{ox1} + C_{si}} \quad (3.249) \]

\[ T_1 = \frac{1 + T_0}{2} \quad (3.250) \]

\[ T_2 = V_{gfb2eff} + T_0 \cdot V_{gfb1eff} + V_t \cdot \left(1 + \frac{C_{ox1}}{C_{ox2}}\right) \quad (3.251) \]

\[ T_3 = \psi_{bs} + \psi_{bd} \quad (3.252) \]

\[ T_4 = \psi_{bd} - \psi_{bs} \quad (3.253) \]

\[ T_5 = V_{gfb2eff} - \frac{T_3}{2} \quad (3.254) \]

\[ T_6 = \frac{T_1 \cdot T_4}{6(T_2 - T_1 T_3)} \quad (3.255) \]

\[ q_{bg} = \frac{C_{ox2}}{C_{ox1}} (T_5 + T_6 T_4 - \Delta V_{th,vbg}) \quad (3.256) \]

\[ q_{d2} = \frac{C_{ox2}}{C_{ox1}} \left[\frac{T_5}{2} + \frac{T_6 T_4}{10} - \frac{T_6}{10(T_2 - T_1 T_3)} (5T_2 - 4T_1 \psi_{bd} - 6T_1 \psi_{bs}) \cdot (T_2 - 2T_1 \psi_{bd})\right] \quad (3.257) \]

3.14.3 Mobility Degradation for C-V Calculation

\[ \eta_{cv} = \begin{cases} \frac{1}{2} & \text{for NMOS} \\ \frac{1}{3} & \text{for PMOS} \end{cases} \quad (3.258) \]

Note: \( \eta \) is used in mobility degradation calculation hence user can tune parameter ETAMOB in I-V fitting while \( \eta_{cv} \) is used in mobility degradation calculation for C-V fitting.

\[ E_{effa,cv} = 10^{-8} \cdot \left(\frac{q_{ba} + \eta_{cv} \cdot q_i}{\epsilon_{ratio} \cdot EOT}\right) \quad (3.259) \]

\[ D_{mob,cv} = 1 + U A(T) \cdot (E_{effa,cv})^{EU} + \frac{UD(T)}{\left(\frac{1}{2} \cdot \left(1 + \frac{q_i}{q_{ba}}\right)CU_{S}(T)\right)} \quad (3.260) \]

\[ D_{mob,CV} = \frac{D_{mob,cv}}{U0MULT} \quad (3.261) \]

3.14.4 Velocity Saturation for C-V Calculation

\[ E_{satCV} = \frac{2 \cdot VSATCV(T) \cdot D_{mob,CV}}{\mu_0(T)} \quad (3.262) \]

\[ E_{satCVL} = E_{satCV} \cdot L_{effCV} \quad (3.263) \]
3.14.5 Channel Length Modulation for C-V Calculation

Channel length modulation causes an effective reduction of the intrinsic capacitance at high drain bias. This reduction factor is modeled by $M_{clm,CV}$:

$$M_{clm,CV} = 1 + \frac{1}{PCLMCV} \ln \left[ 1 + \frac{V_{ds} - V_{ds-eff}}{V_{dsat} + E_{satCVL}} \cdot PCLMCV \right]$$

(3.264)

3.14.6 Assign Variables

$$Q_{fg} = \frac{NF}{M_{clm,CV}} \cdot C_{ox1} \cdot W_{eff} \cdot L_{eff} \cdot q_{fg}$$

(3.265)

$$Q_{bg} = \frac{NF}{M_{clm,CV}} \cdot C_{ox1} \cdot W_{eff} \cdot L_{eff} \cdot q_{bg}$$

(3.266)

$$Q_{d,intrinsic} = \frac{NF}{M_{clm,CV}} \cdot C_{ox1} \cdot W_{eff} \cdot L_{eff} \cdot (-q_{d1} - q_{d2})$$

(3.267)

$$Q_{s,intrinsic} = -Q_{d,intrinsic} - Q_{fg} - Q_{bg}$$

(3.268)

3.15 Parasitic Resistances and Capacitance Models

In this section we will describe the models for parasitic resistances and capacitances in BSIM-IMG.

BSIM-IMG models the parasitic source/drain resistance in two components: a bias-dependent extension resistance and a bias-independent diffusion resistance.

The parasitic capacitance model in BSIM-IMG (adopted from BSIM-CMG) includes a bias-independent outer fringe capacitance, a bias-dependent inner fringe capacitance, a bias-dependent overlap capacitance, and substrate capacitances.

3.15.1 Bias-independent Diffusion Resistance

$R_{s,geo}$ and $R_{d,geo}$ are the source and drain diffusion resistances. The diffusion resistances are simply calculated as the sheet resistance ($R_{SHS}, R_{SHD}$) times the number of squares ($NRS, NRD$):

$$R_{s,geo} = NRS \cdot R_{SHS}$$

(3.269)

$$R_{d,geo} = NRD \cdot R_{SHD}$$

(3.270)
3.15.2 Bias-dependent extension resistance

The bias-dependent extension resistance model is adopted from BSIM4 [6]. There are two options for this bias dependent component. In BSIM3 models $R_{ds}(V)$ is modeled internally through the I-V equation and symmetry is assumed for the source and drain sides. BSIM4 and BSIM-CMG keep this option for the sake of simulation efficiency. In addition, BSIM4 and BSIM-CMG allow the source extension resistance $R_s(V)$ and the drain extension resistance $R_d(V)$ to be external and asymmetric (i.e. $R_s(V)$ and $R_d(V)$ can be connected between the external and internal source and drain nodes, respectively; furthermore, $R_s(V)$ does not have to be equal to $R_d(V)$). This feature makes accurate RF CMOS simulation possible.

The internal $R_{ds}(V)$ option can be invoked by setting the model selector $RDSMOD = 0$ (internal) and the external one for $R_s(V)$ and $R_d(V)$ by setting $RDSMOD = 1$ (external). The expressions for source/drain series resistances are as follows:

**RDSMOD = 0 (Internal)**

$$R_{ds}(V) = \frac{1}{NF \times W_{eff}^{WR}} \cdot \left( RDSWMIN(T) + \frac{RDSW(T)}{1 + PRWG \cdot q_{ia}} \right)$$

$$D_r = 1.0 + NF \times \mu_0(T) \cdot C_{ox1} \cdot \frac{W_{eff}}{L_{eff}} \cdot \frac{i_{ds0}}{\Delta q_i} \cdot \frac{1}{D_{mob} \cdot D_{vsat}} \cdot (R_{ds}(V) + R_{s,geo} + R_{d,geo})$$

$D_r$ goes into the denominator of the final $I_{ds}$ expression.

**RDSMOD = 1 (External)**

$$R_{ds}(V) = 0.0$$

$$V_{gs,eff} = \frac{1}{2} \left[ V_{gs} - V_{fb sd} + \sqrt{(V_{gs} - V_{fb sd})^2 + 10^{-4}} \right]$$

$$V_{gd,eff} = \frac{1}{2} \left[ V_{gd} - V_{fb sd} + \sqrt{(V_{gd} - V_{fb sd})^2 + 10^{-4}} \right]$$

$$R_{source} = \frac{1}{W_{new}^{WR} \cdot NF} \cdot \left( RSWMIN(T) + \frac{RSW(T)}{1 + PRWG \cdot V_{gs,eff}} \right) + R_{s,geo}$$

$$R_{drain} = \frac{1}{W_{new}^{WR} \cdot NF} \cdot \left( RDWMIN(T) + \frac{RDW(T)}{1 + PRWG \cdot V_{gd,eff}} \right) + R_{d,geo}$$

$$D_r = 1.0$$

3.15.3 Overlap Capacitances

$$V_{fgs,ov} = \frac{1}{2} \left[ V_{fgs} - V_{fb sd} + \delta_1 - \sqrt{(V_{fgs} - V_{fb sd} + \delta_1)^2 + 4\delta_1} \right]$$

$$T0 = NF \cdot W_{eff,CV} \cdot LOVS \cdot C_{ox1} \cdot V_{g,es}$$
\[ T_1 = \frac{1}{2} \cdot CKAPPAS \cdot \left[ \sqrt{1 - \frac{4 \cdot V_{fgs}}{CKAPPAS}} - 1 \right] \]  

(3.281)

\[ Q_{fgs,ov} = T_0 + NF \cdot W_{eff,CV} \cdot CGSL \cdot \left\{ V_{fgs} - V_{fbsd} - V_{fgs,ov} - T_1 \right\} \text{devsign} \]  

(3.282)

\[ V_{fgd,ov} = \frac{1}{2} \left[ V_{fgd} - V_{fbsd} + \delta_1 - \sqrt{(V_{fgd} - V_{fbsd} + \delta_1)^2 + 4\delta_1} \right] \]  

(3.283)

\[ T_0 = NF \cdot W_{eff,CV} \cdot LOVD \cdot C_{ox1} \cdot V_{g,ed} \]  

(3.284)

\[ T_1 = \frac{1}{2} \cdot CKAPPAD \cdot \left[ \sqrt{1 - \frac{4 \cdot V_{fgd}}{CKAPPAD}} - 1 \right] \]  

(3.285)

\[ Q_{fgd,ov} = T_0 + NF \cdot W_{eff,CV} \cdot CGDL \cdot \left\{ V_{fgd} - V_{fbsd} - V_{fgd,ov} - T_1 \right\} \cdot \text{devsign} \]  

(3.286)

### 3.15.4 Outer Fringe Capacitances

\[ Q_{fgs,of} = NF \cdot W_{eff,CV} \cdot CFS \cdot V_{g,es} \]  

(3.287)

\[ Q_{fgd,of} = NF \cdot W_{eff,CV} \cdot CFD \cdot V_{g,ed} \]  

(3.288)

### 3.15.5 Source/drain to Substrate Capacitances

\[ C_{sdbgsw0} = CSDBGSW \cdot \ln \left( 1 + \frac{TSI}{EOT2} \right) \]  

(3.289)

\[ Q_{sb} = NF \cdot [C_{ox2} \cdot AS + (PS - W) \cdot C_{sdbgsw0}] \cdot V_{s,bg} \]  

(3.290)

\[ Q_{db} = NF \cdot [C_{ox2} \cdot AD + (PD - W) \cdot C_{sdbgsw0}] \cdot V_{d,bg} \]  

(3.291)

### 3.16 Impact Ionization Current

In a fully-depleted independent double-gate FET, the impact ionization current flows from drain to source,

\[ I_{ii} = \frac{ALPHA_0 + ALPHA_1 \cdot L_{eff}}{L_{eff}} (V_{ds} - V_{dseff}) \cdot e^\frac{-BETA_0}{V_{ds} - V_{dseff}} \cdot I_{ds} \]  

(3.292)

if \( V_{ds} > V_{dseff} \), BETA0 > 0 and \( \frac{ALPHA_0 + ALPHA_1 \cdot L_{eff}}{L_{eff}} > 0 \).
3.17 Gate Induced Source/Drain Leakage

3.17.1 Gate Induced Drain Leakage (GIDL)

\[ I_{gidl} = AGIDL \cdot W_{eff} \cdot NF \cdot \frac{V_{ds} - V_{fgs} - EGIDL + V_{fbsd}}{\varepsilon_{ratio} \cdot EOT1} \cdot \exp \left( -\frac{\varepsilon_{ratio} \cdot EOT1 \cdot BGIDL}{V_{ds} - V_{fgs} - EGIDL + V_{fbsd}} \right) \]  
(3.293)

3.17.2 Gate Induced Source Leakage (GISL) Current

\[ I_{gisl} = AGISL \cdot W_{eff} \cdot NF \cdot \frac{-V_{ds} - V_{fgd} - EGISL + V_{fbsd}}{\varepsilon_{ratio} \cdot EOT1} \cdot \exp \left( -\frac{\varepsilon_{ratio} \cdot EOT1 \cdot BGISL}{-V_{ds} - V_{fgd} - EGISL + V_{fbsd}} \right) \]  
(3.294)

3.18 Front Gate Tunneling Current

Tunneling through the back-gate dielectric is assumed to be negligible.

\[ T_{ox,ratio} = \left( \frac{TOXREF}{TOXP} \right)^{NTOX} \]  
(3.295)

3.18.1 Gate-to-Body current

\( I_{gb} \) is partitioned into a source component, \( I_{gbs} \) and a drain component, \( I_{gbd} \) in this section.

\( I_{gb} \) calculated only if \( IGBMOD = 1 \)

\[ A = 3.75956 \times 10^{-7} \]  
(3.296)

\[ B = 9.82222 \times 10^{11} \]  
(3.297)

\[ V_{aux,igbinv} = NIGBINV \cdot \frac{kT}{q} \cdot \ln \left( 1 + \exp \left( \frac{q_{ia} - EIGBINV}{NIGBINV \cdot kT/q} \right) \right) \]  
(3.298)

\[ I_{gb} = W_{new} \cdot L_{eff} \cdot NF \cdot A \cdot T_{ox,ratio} \cdot V_{gbs} \cdot V_{aux,igbinv} \cdot I_{gtemp} \times \exp \left( -B \cdot TOXP \cdot (AIGBINV - BIGBINV \cdot q_{ia}) \cdot (1 + CIGBINV \cdot q_{ia}) \right) \]  
(3.299)
\[ A = 4.97232 \times 10^{-7} \quad (3.300) \]
\[ B = 7.45669 \times 10^{11} \quad (3.301) \]
\[ V_{fbzb} = \Delta \Phi_1 - E_g/2 - \phi_B \quad (3.302) \]
\[ T_0 = V_{fbzb} - V_{gbg} \quad (3.303) \]
\[ T_1 = T_0 - 0.02; \quad (3.304) \]
\[ V_{aux, igbacc} = NIGBACC \cdot \frac{kT}{q} \cdot \ln \left( 1 + \exp \left( \frac{T_0}{NIGBACC \cdot kT/q} \right) \right) \quad (3.305) \]
\[ V_{oxacc} = \begin{cases} 
0.5 \cdot [T_1 + \sqrt{(T_1)^2 - 0.08 \cdot V_{fbzb}}] & V_{fbzb} \leq 0 \\
0.5 \cdot [T_1 + \sqrt{(T_1)^2 + 0.08 \cdot V_{fbzb}}] & V_{fbzb} > 0 
\end{cases} \quad (3.306) \]
\[ I_{gbacc} = W_{new} \cdot L_{eff} \cdot NF \cdot A \cdot T_{ox, ratio} \cdot V_{gbg} \cdot V_{aux, igbacc} \cdot I_{gtemp} \]
\[ \times \exp (-B \cdot TOXP \cdot (AIGBACC - BIGBACC \cdot V_{oxacc}) \cdot (1 + CIGBACC \cdot V_{oxacc})) \quad (3.307) \]

\( I_g \) mostly flows into the source because the potential barrier for holes is lower at the source, which has a lower potential. To ensure continuity when \( V_{ds} \) switches sign, \( I_g \) is partitioned into a source component, \( I_{gbs} \) and a drain component, \( I_{gbd} \) using a partition function:

\[ T_0 = \tanh \left( \frac{0.6 \cdot q \cdot V_{ds}}{kT} \right) \quad (3.308) \]
\[ W_f = 0.5 + 0.5 \cdot T_0 \quad (3.309) \]
\[ W_r = 0.5 - 0.5 \cdot T_0 \quad (3.310) \]
\[ I_{gbs} = (I_{gbinv} + I_{gbacc}) \cdot W_f \quad (3.311) \]
\[ I_{gbd} = (I_{gbinv} + I_{gbacc}) \cdot W_r \quad (3.312) \]
3.18.2 Gate-to-Channel current

$I_{gc}$ is calculated only for $IGCMOD = 1$

$$A = \begin{cases} 
4.9723 \times 10^{-7} & \text{for NMOS} \\
3.4253 \times 10^{-7} & \text{for PMOS}
\end{cases} \quad (3.313)$$

$$B = \begin{cases} 
7.45669 \times 10^{11} & \text{for NMOS} \\
1.16645 \times 10^{12} & \text{for PMOS}
\end{cases} \quad (3.314)$$

$$T_0 = q_{ia} \cdot (V_{gbg} - 0.5 \cdot V_{dsx} + 0.5 \cdot V_{bgs} + 0.5 \cdot V_{bgd}) \quad (3.315)$$

$$I_{gc0} = W_{new} \cdot L_{eff} \cdot NF \cdot A \cdot T_{ox, ratio} \cdot I_{gtemp} \cdot T_0 \times \exp \left( -B \cdot TOXP \cdot (AIGC - BIGC \cdot q_{ia}) \cdot (1 + CIGC \cdot q_{ia}) \right) \quad (3.316)$$

$$V_{dseffx} = \sqrt{V^2_{dseffx} + 0.01} - 0.1 \quad (3.317)$$

$$I_{gcs} = I_{gc0} \cdot \frac{PIGCD \cdot V_{dseffx} + \exp (PIGCD \cdot V_{dseffx}) - 1.0 + 10^{-4}}{PIGCD^2 \cdot V^2_{dseffx} + 2 \cdot 10^{-4}} \quad (3.318)$$

$$I_{gcd} = I_{gc0} \cdot \frac{1.0 - (PIGCD \cdot V_{dseffx} + 1.0) \exp (-PIGCD \cdot V_{dseffx}) + 10^{-4}}{PIGCD^2 \cdot V^2_{dseffx} + 2 \cdot 10^{-4}} \quad (3.319)$$
3.18.3 Gate-to-Source/Drain current

$I_{gs}, I_{gd}$ are calculated only for $IGCMOD = 1$

$$A = \begin{cases} 
4.97232 \times 10^{-7} & \text{for NMOS} \\
3.42536 \times 10^{-7} & \text{for PMOS} 
\end{cases} \tag{3.320}$$

$$B = \begin{cases} 
7.45669 \times 10^{11} & \text{for NMOS} \\
1.16645 \times 10^{12} & \text{for PMOS} 
\end{cases} \tag{3.321}$$

$$V'_{gs} = \sqrt{V_{gs}^2 + 10^{-4}} \tag{3.322}$$

$$V'_{gd} = \sqrt{V_{gd}^2 + 10^{-4}} \tag{3.323}$$

$$i_{gsd,mult} = Igtemp \cdot \frac{W_{\text{new}} \cdot A}{(TOXP \cdot POXEDGE)^2} \cdot \left(\frac{TOXREF}{TOXP \cdot POXEDGE}\right)^{NTOX} \tag{3.324}$$

$$I_{gs} = NF \cdot i_{gsd,mult} \cdot DLCIGS \cdot V_{gs} \cdot V'_{gs} \times \exp\left(-B \cdot TOXP \cdot POXEDGE \cdot (AIGS - BIGS \cdot V'_{gs}) \cdot (1 + CIGS \cdot V'_{gs})\right) \tag{3.325}$$

$$I_{gd} = NF \cdot i_{gsd,mult} \cdot DLCIGD \cdot V_{gd} \cdot V'_{gd} \times \exp\left(-B \cdot TOXP \cdot POXEDGE \cdot (AIGD - BIGD \cdot V'_{gd}) \cdot (1 + CIGD \cdot V'_{gd})\right) \tag{3.326}$$
3.19 Gate Resistance Network Model

3.19.1 General Description and Schematic

BSIM6 provides two options for modeling gate electrode resistance. The model selector RGATE-MOD is used to choose different options.

![Gate resistance network for RGATE-MOD = 0](image1)

Figure 5: Gate resistance network for RGATE-MOD = 0

![Gate resistance network for RGATE-MOD = 1](image2)

Figure 6: Gate resistance network for RGATE-MOD = 1

3.19.2 Model Options

There are two model selectors for gate resistance network.

**RGATE-MOD = 0** (zero-resistance): In this case, no gate resistance is generated (see Figure 5).

**RGATE-MOD = 1** (constant-resistance): In this case, only the electrode gate resistance (bias-independent) is generated by adding an internal gate node (see Figure 6). \( R_{geltd} \) is given by

\[
R_{geltd} = \frac{R_{SHG} \cdot (X_{GW} + \frac{W_{eff}}{3 \cdot NGCON})}{NGCON \cdot (L_{eff} - X_{GL}) \cdot NF}
\]  

(3.328)
3.20 Self-Heating Model

The self-heating effect is modeled using an R-C network approach (based on BSIMSOI [9]), as illustrated in figure 7. The voltage at the temperature node (T) is used for all temperature-dependence calculations in the model. The total temperature (T) used in the model is ambient temperature (T) plus the $\Delta T_{SHE}$ computed on the temperature node (T).

**Thermal resistance and capacitance calculations**

The thermal resistance ($R_{th}$) and capacitance ($C_{th}$) are modified from BSIMSOI to capture the width dependence.

\[
\frac{1}{R_{th}} = G_{th} = \frac{WTH0 + W_{eff}}{RTH0} \cdot NF \quad (3.329)
\]

\[
C_{th} = CTH0 \cdot (WTH0 + W_{eff}) \cdot NF \quad (3.330)
\]
3.21 Noise Modeling

The following noise sources in MOSFETs are modeled in BSIM4 [6] for SPICE noise analysis: flicker noise (also known as 1/f noise), channel thermal noise and induced gate noise.

Table 3.21 lists the origin of each noise model:

<table>
<thead>
<tr>
<th>Noise models in BSIM-IMG102.6.0</th>
<th>Origin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flicker noise model</td>
<td>BSIM4 Unified Model (FNOIMOD=1)</td>
</tr>
<tr>
<td>Thermal noise</td>
<td>BSIM4 (TNOIMOD=0)</td>
</tr>
<tr>
<td>Gate current shot noise</td>
<td>BSIM4 gate current noise</td>
</tr>
</tbody>
</table>

3.21.1 Flicker Noise Model

BSIM-IMG102.6.0 flicker noise model is same as FNOIMOD=1 in BSIM4. The unified physical flicker noise model is smooth over all bias regions. The physical mechanism for the flicker noise is trapping/detrapping-related charge fluctuation in oxide traps, which results in fluctuations of both mobile carrier numbers and mobilities in the channel. The unified flicker noise model captures this physical process. In the inversion region, the noise density is expressed as [10]

\[
E_{sat, noi} = \frac{2 \cdot VSAT(T)}{\mu_0(T)D_{mobs}}
\]  

(3.331)

\[
L_{eff, noi} = L_{eff} - 2 \cdot LINTNOI
\]  

(3.332)

\[
\Delta L_{clm} = l \cdot \ln \left[ \frac{1}{E_{sat, noi}} \cdot \left( \frac{V_{ds} - V_{dseff}}{l} + EM \right) \right]
\]  

(3.333)

where \( L_{eff, noi} = L_{eff} - 2 \cdot LINTNOI \), \( \mu_0(T) \) is the effective mobility at the given bias condition, and \( L_{eff} \) and \( W_{eff} \) are the effective channel length and width, respectively. The parameter \( N_0 \) is the charge density at the source side given by

\[
N_0 = \frac{C_{ox1} \cdot q_{is}}{q}
\]  

(3.334)

The parameter \( N_l \) is the charge density at the drain end given by

\[
N_l = \frac{C_{ox1} \cdot q_{id}}{q}
\]  

(3.335)

and \( N^* \) is given by

\[
N^* = \frac{kT}{q^2} (C_{ox1} + CIT)
\]  

(3.336)
where CIT is a model parameter from DC IV.

\[ FN_1 = NOIA \cdot \ln \left( \frac{N_0 + N^*}{N_t + N^*} \right) + NOIB \cdot (N_0 - N_t) + \frac{NOIC}{2} (N_0^2 - N_t^2) \]  

\[ FN_2 = \frac{NOIA + NOIB \cdot N_t + NOIC \cdot N_t^2}{(N_t + N^*)^2} \]  

(3.337)  
(3.338)

In the strong inversion region, the noise density is written as

\[ S_{si} = \frac{kTq^2 \mu_0(T)I_{ds}}{C_{ox} L_{eff, noi} \cdot 10^{10}} \cdot FN_1 + \frac{kT I_{ds}^2 \Delta L_{c_{tm}}}{W_{eff} \cdot NF \cdot L_{eff, noi} \cdot 10^{10}} \cdot FN_2 \]  

(3.339)

In the subthreshold region, the noise density is written as

\[ S_{wi} = \frac{NOIA \cdot kT \cdot I_{ds}^2}{W_{eff} \cdot NF \cdot L_{eff, noi} \cdot 10^{10} \cdot N^*} \]  

(3.340)

The total flicker noise density is

\[ S_{id, flicker} = \frac{S_{wi} S_{si}}{S_{wi} + S_{si}} \]  

(3.341)

### 3.21.2 Thermal Noise Model

Charge-based model (default model) similar to that used in BSIM3v3.2 and BSIM4.7.0 (TNOIMOD=0) is modeled. The noise current is given by

\[ Q_{inv} = |Q_{s,intrinsic} + Q_{d,intrinsic}| \]  

(3.342)

\[ \frac{\sqrt{I_d^2}}{I_d} = \begin{cases} 
NTNOI \cdot \frac{4kT \Delta f}{R_{ds}(V) + L_{eff, noi}^2} & \text{if } RDSMOD = 0 \\
NTNOI \cdot \frac{4kT \Delta f}{L_{eff, noi}^2} \cdot \mu_0(T)Q_{inv} & \text{if } RDSMOD = 1 
\end{cases} \]  

(3.343)

where \( R_{ds}(V) \) is the bias-dependent LDD source/drain resistance, and the parameter NTNOI is introduced for more accurate fitting of short-channel devices. \( Q_{inv} \) is the total inversion charge in the channel. \( Q_{s,intrinsic}, Q_{d,intrinsic} \) are intrinsic charges at source/drain ends.
Gate current shot noise

\[
\overline{i_{gs}^2} = 2q(I_{gcs} + I_{gs} + I_{gbs}) \tag{3.344}
\]

\[
\overline{i_{gd}^2} = 2q(I_{gcd} + I_{gd} + I_{gbd}) \tag{3.345}
\]

### 3.21.3 Resistor Noise Model

The noise associated with each parasitic resistors in BSIM-IMG are calculated

If \( RDSMOD = 1 \) then

\[
\frac{\overline{i_{RS}^2}}{\Delta f} = 4kT \cdot \frac{1}{R_{source}} \tag{3.346}
\]

\[
\frac{\overline{i_{RD}^2}}{\Delta f} = 4kT \cdot \frac{1}{R_{drain}} \tag{3.347}
\]

If \( RGATEMOD = 1 \) then

\[
\frac{\overline{i_{RG}^2}}{\Delta f} = 4kT \cdot \frac{1}{R_{geltd}} \tag{3.348}
\]
4 Model Calibration Introduction

The objective of this section is to provide guidelines for the extraction of the main model parameters. The procedure is structured in such a way that parameters linked to specific psychical phenomena are extracted from analyses where these effects are prominent. Although parameter extraction is not always a straightforward procedure, the aim is to minimize the effort invested and the number of the essential loops performed. If all the steps of the described procedure are followed then a global model card is obtained which means that the model can be used across the entire width/length plane of the technology.

Before proceeding to the extraction of any parameter, it is very important that $TNOM$ is set to the value of the temperature at which the nominal measurements were carried out. Biases in extraction steps using N-type bias convention. P-type can be performed using reverse sign conventions.

5 Global Parameter Extraction

The objective of this procedure is to find one global set of parameters for BSIM-IMG to fit experimental data for devices with channel length ranging from short to long dimensions. Some parameters are measured or specified by user, and need not be extracted, such as those given in Table 1.

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EPSROX</td>
<td>Relative Gate Dielectric Constant</td>
</tr>
<tr>
<td>EPSRSUB</td>
<td>Relative Dielectric Constant of the Channel</td>
</tr>
<tr>
<td>EOT1</td>
<td>Electrical Gate Equivalent Oxide Thickness of Front Gate</td>
</tr>
<tr>
<td>EOT2</td>
<td>Electrical Gate Equivalent Oxide Thickness of Back Gate</td>
</tr>
<tr>
<td>NBODY</td>
<td>Channel Doping Concentration</td>
</tr>
<tr>
<td>NSD</td>
<td>S/D Doping Concentration</td>
</tr>
<tr>
<td>XW/XL</td>
<td>Channel W/L Offset due to Mask/Etch Effect</td>
</tr>
<tr>
<td>L</td>
<td>Designed Gate Length</td>
</tr>
<tr>
<td>W</td>
<td>Designed Gate Width</td>
</tr>
<tr>
<td>NF</td>
<td>Number of Fingers in parallel</td>
</tr>
<tr>
<td>GIDLMOD</td>
<td>0: off 1:on</td>
</tr>
<tr>
<td>RDSMOD</td>
<td>0: fixed bias dependence, 1: external bias dependence</td>
</tr>
<tr>
<td>TYPE</td>
<td>-1: PMOS 1:N莫斯</td>
</tr>
</tbody>
</table>
Now we start extracting all the global parameters. The extraction procedure can be divided into 6 stages:

- Gate Capacitance Fitting ($C_{GG}$ vs $V_{GS}$)
- Gate Current Fitting ($I_{GS}$ vs $V_{GS}$)
- Drain Current Fitting ($I_{DS}$ vs $V_{GS}$) in Linear region
- Drain Current Fitting ($I_{DS}$ vs $V_{GS}$) in Saturation region
- Drain Current Fitting ($I_{DS}$ vs $V_{DS}$)
- Drain Current Fitting ($I_{DS}$ vs $V_{DS}$) for threshold voltage sensitivity to back gate voltage

5.1 Extraction of Long Channel and Long Width Device Parameters

5.1.1 Long Channel Gate Capacitance Fitting: ($C_{GG}$ vs $V_{GS}$) @ $V_{DS} = 0$ V & $V_{BG} = 0$ V

Step 1: At this step, process parameters and parameters related to quantum mechanical effect are extracted. Even if values have been already assigned to process parameters, a fine tuning should be made in order to fit accurately the electrical behavior of the device. From $C_{GG}$ vs $V_{GS}$ curve, the following process parameters can be extracted: $NBODY$, $EOT1$, $EOT2$ and $NGATE$, $PHIG1$, $PHIG2$. Each of these parameters affects a different region or in a different way the $C_{GG}$ capacitance, so they should be extracted accordingly. More specifically:

- $NBODY$ is affecting $C_{GG}$ in the depletion region/weak inversion region.
- $EOT1$ and $EOT2$ are defined as physical gate equivalent oxide thickness for front/back gates.

Furthermore, the value of front gate capacitance $C_{OX}$ is affected by the Quantum Mechanical effect. So, the parameters: $PQM$, $QM0$ and $ETAQM$ are also extracted from $C_{GG}$ vs $V_{GS}$ analysis, when focusing at the slope of $C_{GG}$ at the onset of the strong-inversion region.
5.1.2 Long Channel Drain Current Fitting: $I_{DS}$ vs $V_{GS}$ Analysis in Linear Region

Step 2: In this step, the $V_G$ dependence of the drain current $I_{DS}$, is extracted. Carrier mobility and interface charge related parameters are extracted.

<table>
<thead>
<tr>
<th>Extracted Parameters</th>
<th>Device &amp; Experimental Data</th>
<th>Extraction Methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIT, CDSC</td>
<td>Long device $I_{DS}$ vs $V_{GS}$ @ $V_{DS} = 0.05V$ @ $V_{BG} = 0.0V$</td>
<td>Observe sub-threshold region offset and slope.</td>
</tr>
<tr>
<td>CBGCBG0, CBGCBG</td>
<td>Long device $I_{DS}$ vs $V_{GS}$ @ $V_{DS} = 0.05V$ @ $V_{BG} = 0.0V$</td>
<td>Observe sub-threshold region offset and slope.</td>
</tr>
<tr>
<td>$U_0$, $U_A$, $U_D$, $U_C$</td>
<td>Long device $I_{DS}$ vs $V_{DS}$ @ $V_{DS} = 0.05V$ @ $V_{BG} = 0.0V$</td>
<td>Observe strong inversion region $I_{Dlin}$ and $g_{mlin}$.</td>
</tr>
</tbody>
</table>

Note: 0 subscript denotes nominal T (300K).

5.1.3 Long Channel Drain Current Fitting: $I_{DS}$ vs $V_{GS}$ Analysis in Saturation Region

Step 3: Tune DIBL parameters.

<table>
<thead>
<tr>
<th>Extracted Parameters</th>
<th>Device &amp; Experimental Data</th>
<th>Extraction Methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>ETA0, DSUB, CDSCD</td>
<td>Long devices $I_{DS}$ vs $V_{GS}$ @ $V_{DS} = V_{dd}$ @ $V_{BG} = 0.0V$</td>
<td>Observe sub-threshold region of all devices in the same plot.</td>
</tr>
<tr>
<td>ETAB, CBGCBGD</td>
<td>Short and long devices $I_{DS}$ vs $V_{GS}$ @ $V_{GS} = V_{DS} = V_{dd}$ @ $V_{BG} = 0.0V$</td>
<td>Observe sub-threshold region offset and slope.</td>
</tr>
</tbody>
</table>

Note: Velocity saturation, smoothing function and output conductance parameters are tuned for better fitting.

Step 4: Extract velocity saturation parameters for long gate lengths, see short channel effects section.

<table>
<thead>
<tr>
<th>Extracted Parameters</th>
<th>Device &amp; Experimental Data</th>
<th>Extraction Methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>$VSAT$, $PTWG$, $KSATIV$, $MEXP$</td>
<td>Long device and medium devices $I_{DS}$ vs $V_{GS}$ @ $V_{DS} = V_{dd}$ @ $V_{BG} = 0.0V$</td>
<td>Observe strong inversion region $I_{Dsat}$, $g_{msat}$.</td>
</tr>
<tr>
<td>$VSATB$, $PTWGB$, $PTWGB2$</td>
<td>Long device and medium devices $I_{DS}$ vs $V_{GS}$ @ $V_{DS} = V_{dd}$ @ $V_{BG} = 0.0V$</td>
<td>Observe strong inversion region $I_{Dsat}$, $g_{msat}$.</td>
</tr>
</tbody>
</table>

Note: long channel alone is not enough to accurately extract velocity saturation parameters.
Step 5: Extract output conductance parameters.

<table>
<thead>
<tr>
<th>Extracted Parameters</th>
<th>Device &amp; Experimental Data</th>
<th>Extraction Methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEXP, PCLM, PDIBL1, PDIBL2, DROUT, PVAG</td>
<td>Long and short devices $I_{DS}$ vs $V_{DS}$ @ different $V_{GS}$ @ $V_{BG} = 0.0V$</td>
<td>Observe strong inversion region $I_{DS}$ vs $V_{DS}$ &amp; $g_{DS}$ vs $V_{DS}$ @ different $V_{GS}$ @ $V_{BG} = 0.0V$.</td>
</tr>
</tbody>
</table>

5.1.4 Drain Current Fitting ($I_{DS}$ vs $V_{DS}$) for Threshold Voltage Sensitivity to Back Gate Voltage

Threshold voltage of the FDSOI transistor is extracted from constant current method. To calibrate $V_{th}$ vs back gate voltage $V_{bgs}$, start with BPFACTORPW (or BPFACTORNW for N-type back gate) equal to zero which means no back gate depletion effect is considered. Calibrate $V_{th}$ data for positive $V_{bgs}$ for p-type substrate (or equivalently, $V_{th}$ data for negative $V_{bgs}$ for n-type substrate). See Figure 8.

If the measured data show a deviation from an straight line due to back gate depletion, 1) set VKNEE1PW (or VKNEE1NW) equal to the back gate voltage at which the lines depart and 2) start increasing BPFACTORPW (or BPFACTORNW) and adjusting VKNEE2PW (or VKNEE2NW) for a good fit. See Figure 9.

![Figure 8: $V_{th}$ vs back gate voltage $V_{bgs}$, NMOS with p-type substrate (p-well). The back gate depletion effect is turned off in the model.](image-url)
Figure 9: $V_{th}$ vs back gate voltage $V_{bg}$, NMOS with p-substrate (well), including back gate depletion effect.

5.2 Extraction of Short Channel Effects & Length Scaling Parameters

5.2.1 Short Channel Gate Capacitance Fitting: ($C_{GG}$ vs $V_{GS}$) @ $V_{DS} = 0$ V & $V_{BG} = 0$ V

Step 6: In this step, parameters related to overlap and fringing capacitances are extracted. More specifically:

• Extraction of parameters related to overlap and fringing capacitances is carried out by studying the entire range of $V_{GS}$ bias of $C_{GG}$ vs $V_{GS}$ characteristic. These parameters are: CGSL, CGDL, CKAPPAS, CKAPPAD, CGSL, CGDL, CKAPPAS and CKAPPAD are extracted from $C_{GD}$ vs $V_{GS}$ at high $V_{BG}$ (when S, D and B terminals are connected together).

• DLC, which is the channel-length offset parameter for the CV model, is extracted in the strong-inversion region of $C_{GG}$.

A sample global fitting for C-V characteristics of NMOS and PMOS device is shown in Figure 10.
Figure 10: $C_{GG}$ vs $V_{GS} @ V_{DS} = 0.05V$ and $V_{BG} = 0.0V$, Symbols: Data [11], Lines: the BSIM-IMG model.

5.2.2 Short Channel Drain Current Fitting: $I_{DS}$ vs $V_{GS}$ Analysis in Linear Region

Step 7: Tune $V_{th}$ roll-off, DIBL and SS degradation parameters.

<table>
<thead>
<tr>
<th>Extracted Parameters</th>
<th>Device &amp; Experimental Data</th>
<th>Extraction Methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>DVT0, DVT1, CDSC</td>
<td>Both short and medium devices $I_{DS}$ vs $V_{GS} @ V_{DS} = 0.05V @ V_{BG} = 0.0V$</td>
<td>Observe sub-threshold region of all devices in the same plot. Optimize DVT0, DVT1, CDSC.</td>
</tr>
</tbody>
</table>

Step 8: Extract low field mobility $U_0[L]$ for long and medium gate lengths. So far, we have good fit with data in sub-threshold regions from long to short channel devices, and strong inversion for long channel devices. We need good fit for strong inversion in medium and short channel devices. In linear region, current is to the first order, governed by low field mobility. So we start by tuning low field mobility values. In short channel devices series resistance and enhanced mobility degradation effects are pronounced. To avoid the influence of these effects, long and medium channel length devices are selected to especially extract low field mobility parameters.

<table>
<thead>
<tr>
<th>Extracted Parameters</th>
<th>Device &amp; Experimental Data</th>
<th>Extraction Methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>UP, LPA</td>
<td>Long and medium devices $I_{DS}$ vs $V_{GS} @ V_{DS} = 0.05V @ V_{BG} = 0.0V$</td>
<td>Observe strong inversion region $I_{D_{lin}}$ and $g_{mlin}$, extract $U_0[L]$ to get UP, LP.</td>
</tr>
</tbody>
</table>
Step 9: Extract mobility and series resistance parameters for short gate lengths.

<table>
<thead>
<tr>
<th>Extracted Parameters</th>
<th>Device &amp; Experimental Data</th>
<th>Extraction Methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>AParam (i.e., AUA, AEU, AUC, AUD, AUDB, ARDSW, ARSW, ARDW), BParam (i.e., BUA, BEU, BUC, BUD, BUDB, BRDSW, BRSW, BRDW), LINT, LL, LLN</td>
<td>Short and medium devices $I_{DS}$ vs $V_{GS} @ V_{DS} = 0.05V @ V_{BG} = 0.0V$</td>
<td>a. Observe strong inversion region $I_{dlin}$ and $g_{mlin}$. Similar to Step 8, find values of UA, UD, RDSW that gives good fit to experimental data, varying them simultaneously. $UA_0$, $UD_0$ are provided from Step 2 and LINT is provided from parameter Initialization.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>b. Variation of each parameter with respect to $L$ should be kept minimal with smooth continuous trend.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>c. From the length dependence of UA, UD, RDSW and L, find AUA, BUA, AUD, BUD, ARDSW, BRDSW, LL, LLN.</td>
</tr>
</tbody>
</table>

**Note:** Step 8 parameters are extracted from long and medium channel lengths, whereas, Step 9 involves short and medium channel lengths. Thus, the extracted parameters remain valid for all channel lengths to bring forth the intended length dependence in effect.

Step 10: Tune geometry scaling parameters for mobility degradation parameters.

<table>
<thead>
<tr>
<th>Refined Parameters</th>
<th>Device &amp; Experimental Data</th>
<th>Extraction Methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>AUA, AUD, ARDSW, LL</td>
<td>Short and medium devices $I_{DS}$ vs $V_{GS} @ V_{DS} = 0.05V$, @ $V_{BG} = 0.0V$</td>
<td>Observe strong inversion region of all devices in the same plot; optimize AUA, AUD, ARDSW, LL.</td>
</tr>
</tbody>
</table>

Step 11: Further optimize the parameters by repeating step 10 and 7. If not getting good fitting, tune LLN, BUA, BUD, BRDSW. Iteration ends in step 10 and then proceeds to step 12.
5.2.3 Short Channel Drain Current Fitting: $I_{DS}$ vs $V_{GS}$ Analysis in Saturation Region

Step 12: Extract velocity saturation parameters for short and medium gate lengths

<table>
<thead>
<tr>
<th>Extracted Parameters</th>
<th>Device &amp; Experimental Data</th>
<th>Extraction Methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVSAT, AVSAT1, APTWG, BVSAT, BVSAT1, BPTWG</td>
<td>short and medium devices $I_{DS}$ vs $V_{GS}$ @ $V_{DS} = V_{dd}$, @ $V_{BG} = 0.0V$</td>
<td>a. Observe strong inversion region of $I_{Dsat}$ and $g_{msat}$. Find VSAT1, VSAT, PTWG, AVSAT1, BVSAT1, AVSAT, BVSAT, APTWG, BPTWG to fit data.</td>
</tr>
</tbody>
</table>

Step 13: Tune geometry scaling parameters for velocity saturation, over the range from short to long channel devices.

<table>
<thead>
<tr>
<th>Refined Parameters</th>
<th>Device &amp; Experimental Data</th>
<th>Extraction Methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVSAT, AVSAT1, APTWG</td>
<td>medium and short devices $I_{DS}$ vs $V_{GS}$ @ $V_{DS} = V_{dd}$, @ $V_{BG} = 0.0V$</td>
<td>Observe strong inversion region of all devices in the same plot. Optimize AVSAT, AVSAT1, APTWG.</td>
</tr>
</tbody>
</table>

5.2.4 Other Parameters Representing Important Physical Effects

Step 14: Extract GIDL current model parameters.

<table>
<thead>
<tr>
<th>Extracted Parameters</th>
<th>Device &amp; Experimental Data</th>
<th>Extraction Methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>AGIDL, BGIDL, EGIDL</td>
<td>long and short devices $I_{DS}$ vs $V_{DS}$ @ different $V_{GS}$ @ $V_{BG} = 0.0V$</td>
<td>Observe sub-threshold region $I_{DS}$ vs $V_{GS}$ @ $V_{DS} = V_{dd}$ &amp; $R_{out}$ vs $V_{DS}$ @ $V_{GS} &lt; 0V$ and $V_{GS} = 0V$.</td>
</tr>
</tbody>
</table>

5.2.5 Smoothing between Linear and Saturation Regions

Step 15: Extract geometry scaling parameters for smoothing function parameter.

<table>
<thead>
<tr>
<th>Extracted Parameters</th>
<th>Device &amp; Experimental Data</th>
<th>Extraction Methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEXP, AMEXP, BMEXP</td>
<td>long and short devices $I_{DS}$ vs $V_{DS}$ @ different $V_{GS}$</td>
<td>Observe data trend; extract AM-EXP and BMEXP.</td>
</tr>
</tbody>
</table>

A sample global fitting for long channel and short channel PMOS device is shown in Figure 11. See the length scaling extraction overview flow chart for details in Figure 12.
5.3 Extraction of Narrow Channel Effects & Width Scaling Parameters

The next step in the parameter extraction procedure is the extraction of the parameters that are either related to narrow channel effects or express the different width dependencies. So at this part, devices across the entire width range of the technology, from the narrowest to the widest one, are studied simultaneously. A full range of W-binning model parameters is listed in section 6.2 (see terms with small b superscript). In order to avoid the impact of short channel effects or the length dependencies these devices should have the same long channel. The extraction that is carried out follows the same flow as in Figure 12, but now a set of devices with constant long channel but different channel widths is used.

5.3.1 Gate Capacitance $C_{GG}$ vs $V_{GS}$ Analysis @ $V_S = 0$ V, $V_D = 0$ V & $V_{BG} = 0$ V

In this step, parameters related to the width dependencies of the CV behavior of the device are extracted. More specifically:

- **DWC**, which is the channel-width offset parameter for the CV model, is extracted in the strong-inversion region of $C_{GG}$.
- **LWLC** and **WWLC**, which are coefficients of length/width dependencies for CV model, are extracted in the strong-inversion region of $C_{GG}$.

5.3.2 Drain Current $I_D$ vs $V_{GS}$ Analysis @ $V_{DS} = [V_{D,lin}, V_{D,sat}]$, $V_S = 0$ V & $V_{BG} = 0$ V

In this step, geometry dependent parameters for modeling $I_{DS}$ of the narrow/short channel devices, are extracted. Similar to the procedure described in Figure 12, the parameters are divided in two
groups, those which are extracted in linear mode (i.e. $V_D \ll V_G - V_{th}$) and those which are extracted in saturation (i.e. $V_D \gg V_G - V_{th}$). It is very important that during the extraction both $I_D$ and $g_m$ of all the devices are studied at once. Parameter $WINT$ is the channel width offset parameter and is used to fit both the sub-threshold slope and the $V_{th}$ across $W$.

## 5.4 Other Effects

Step 16: Temperature and Self-Heating Effects.

<table>
<thead>
<tr>
<th>Extracted Parameters</th>
<th>Device &amp; Experimental Data</th>
<th>Extraction Methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal resistance (RTH0) and capacitances (CTH0) for the self-heating model and etc.</td>
<td>$I_{DS}$ vs $V_{GS}$ @ $V_{DS} = V_{dd}$ under different temperatures.</td>
<td>Observe data trend and tune RTH0, CTH0.</td>
</tr>
</tbody>
</table>

Step 17: Gate leakage current

<table>
<thead>
<tr>
<th>Extracted Parameters</th>
<th>Device &amp; Experimental Data</th>
<th>Extraction Methodology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate tunneling current parameters.</td>
<td>$I_{GC}$ vs $V_{GS}$ @ $V_{DS} = 0V$.</td>
<td>Observe data trend and tune NIGCINV, AIGCINV, BIGCINV, CIGCINV, EIGCINV etc.</td>
</tr>
</tbody>
</table>
Figure 12: Parameters Extraction Procedure in BSIM-IMG Model.
6 Node Description and Complete Parameter List

6.1 Node name and Description

Mname < D node> < FG node> < S node> < BG node>

Description

<D node> : Drain node
<FG node> : Front-Gate node
<S node> : Source node
<BG node> : Back-Gate node

6.2 Instance Parameters

Note: Instance parameters with superscript \(^{(m)}\) are also model parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Unit</th>
<th>Default</th>
<th>Min</th>
<th>Max</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>L(^{(m)})</td>
<td>m</td>
<td>30n</td>
<td>1n</td>
<td>-</td>
<td>Designed Gate Length</td>
</tr>
<tr>
<td>W</td>
<td>m</td>
<td>1e-6</td>
<td>1n</td>
<td>-</td>
<td>Designed Gate Width</td>
</tr>
<tr>
<td>NF</td>
<td>-</td>
<td>1</td>
<td>1</td>
<td>-</td>
<td>Number of fingers</td>
</tr>
<tr>
<td>AS(^{(m)})</td>
<td>m(^2)</td>
<td>0</td>
<td>0</td>
<td>-</td>
<td>Source to substrate overlap area through oxide (all fingers)</td>
</tr>
<tr>
<td>AD(^{(m)})</td>
<td>m(^2)</td>
<td>0</td>
<td>0</td>
<td>-</td>
<td>Drain to substrate overlap area through oxide (all fingers)</td>
</tr>
<tr>
<td>PS(^{(m)})</td>
<td>m</td>
<td>0</td>
<td>0</td>
<td>-</td>
<td>Perimeter of source to substrate overlap region through oxide (all fingers)</td>
</tr>
<tr>
<td>PD(^{(m)})</td>
<td>m</td>
<td>0</td>
<td>0</td>
<td>-</td>
<td>Perimeter of drain to substrate overlap region through oxide (all fingers)</td>
</tr>
<tr>
<td>NRS(^{(m)})</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>-</td>
<td>Number of source diffusion squares (RGEOMOD = 0)</td>
</tr>
<tr>
<td>NRD(^{(m)})</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>-</td>
<td>Number of drain diffusion squares (RGEOMOD = 0)</td>
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Note: Parameters for global variability modeling

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<tr>
<td>XL</td>
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<td>L offset for channel length due to mask/etch effect</td>
</tr>
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<td>DTEMP</td>
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<td>0</td>
<td>-</td>
<td>-</td>
<td>Variability handle for temperature</td>
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<tr>
<td>DELVTRAND</td>
<td>V</td>
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<td>-</td>
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<td>Variability in Vth</td>
</tr>
<tr>
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<td>Variability in carrier mobility</td>
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### 6.3 Model Controllers and Process Parameters

Note: binnable parameters are marked as: \(^{(b)}\)

<table>
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<tr>
<td>TYPE</td>
<td>-</td>
<td>NMOS</td>
<td>PMOS</td>
<td>NMOS</td>
<td>(\text{NMOS=1, PMOS=-1})</td>
</tr>
<tr>
<td>WELTYPE</td>
<td>-</td>
<td>p-well</td>
<td>p-well</td>
<td>n-well</td>
<td>(\text{n-well=1, p-well=-1})</td>
</tr>
<tr>
<td>CHARGEMOD</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Selects the inversion charge density model for the body; 0= simplified, 1= more accurate</td>
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<tr>
<td>RDSMOD</td>
<td>-</td>
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<td>0</td>
<td>1</td>
<td>bias-dependent source/drain resistance model selector (controls (si) and (di) nodes); 0 = internal, 1 = external</td>
</tr>
<tr>
<td>IGCMOD</td>
<td>-</td>
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<td>1</td>
<td>model selector for (I_{gc}), (I_{gs}) and (I_{gd}); 1=turn on, 0=turn off</td>
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<td>IGBMOD</td>
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<td>0</td>
<td>1</td>
<td>model selector for (I_{gb}); 1=turn on, 0=turn off</td>
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<td>GIDLMOD</td>
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<td>GIDL/GISL current switcher; 1=turn on, 0=turn off</td>
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<td>Self-heating mode switch; 1=turn on, 0=turn off</td>
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<td>RGATEMOD</td>
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<td>-</td>
<td>Gate resistance model selector; 1=turn on, 0=turn off</td>
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<td>NFMOD</td>
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<td>-</td>
<td>Number of Finger selector; 1=W taken as single finger width, 0=W taken as total width like BSIM4</td>
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<td>CHARGEWF</td>
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<td>-</td>
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<td>Average Channel Charge Weighting Factor, +1:source-side, 0:middle, -1:drain-side</td>
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<td>XW</td>
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<td>LL</td>
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<tr>
<td>Name</td>
<td>Unit</td>
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<td>Max</td>
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<td>Length reduction parameter (dopant diffusion effect)</td>
</tr>
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<td>LLC</td>
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<td>-</td>
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<td>LWC</td>
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<td>Length scaling parameter</td>
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<tr>
<td>WLC</td>
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<td>-</td>
<td>Width scaling parameter</td>
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<tr>
<td>WWC</td>
<td>(m)</td>
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<td>-</td>
<td>Width scaling parameter</td>
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<tr>
<td>WWLC</td>
<td>(m)</td>
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<td>-</td>
<td>Width scaling parameter</td>
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<tr>
<td>EOT1</td>
<td>(m)</td>
<td>1.0(\times) 10(^{-11})</td>
<td>0.1(\times) 10(^{-11})</td>
<td>-</td>
<td>SiO(_2) equivalent front gate dielectric thickness (including inversion layer thickness)</td>
</tr>
<tr>
<td>EOT2</td>
<td>(m)</td>
<td>140(\times) 10(^{-11})</td>
<td>0.1(\times) 10(^{-11})</td>
<td>-</td>
<td>SiO(_2) equivalent back gate dielectric thickness (including back gate depletion layer thickness)</td>
</tr>
<tr>
<td>EOT1P</td>
<td>(m)</td>
<td>EOT1</td>
<td>0.1(\times) 10(^{-11})</td>
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<td>physical front gate dielectric thickness for CV</td>
</tr>
<tr>
<td>DTOX1</td>
<td>(m)</td>
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<td>-</td>
<td>-</td>
<td>Difference between effective dielectric thickness and physical thickness</td>
</tr>
<tr>
<td>TSI</td>
<td>(m)</td>
<td>8(\times) 10(^{-8})</td>
<td>1(\times) 10(^{-8})</td>
<td>-</td>
<td>body thickness</td>
</tr>
<tr>
<td>NBODY(^{(b)})</td>
<td>(m^{-3})</td>
<td>1(\times) 10(^{22})</td>
<td>1(\times) 10(^{18})</td>
<td>5(\times) 10(^{24})</td>
<td>Channel doping concentration</td>
</tr>
<tr>
<td>NBG</td>
<td>(m^{-3})</td>
<td>5(\times) 10(^{23})</td>
<td>-</td>
<td>-</td>
<td>well or back gate doping level, zero for metal back gate</td>
</tr>
<tr>
<td>EASUB</td>
<td>eV</td>
<td>4.05</td>
<td>0</td>
<td>-</td>
<td>electron affinity of the substrate material</td>
</tr>
<tr>
<td>NI0SUB</td>
<td>(m^{-3})</td>
<td>1.1(\times) 10(^{16})</td>
<td>-</td>
<td>-</td>
<td>intrinsic carrier concentration of channel at 300.15K</td>
</tr>
<tr>
<td>BG0SUB</td>
<td>eV</td>
<td>1.12</td>
<td>-</td>
<td>-</td>
<td>band gap of the channel material at 300.15K</td>
</tr>
<tr>
<td>NC0SUB</td>
<td>(m^{-3})</td>
<td>2.86(\times) 10(^{25})</td>
<td>-</td>
<td>-</td>
<td>conduction band density of states at 300.15K</td>
</tr>
<tr>
<td>Name</td>
<td>Unit</td>
<td>Default</td>
<td>Min</td>
<td>Max</td>
<td>Description</td>
</tr>
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<td>----------</td>
<td>---------</td>
<td>-----</td>
<td>-----</td>
<td>------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>PHIG1 (^{(b)})</td>
<td>V</td>
<td>4.61</td>
<td>-</td>
<td>-</td>
<td>Workfunction of the front gate</td>
</tr>
<tr>
<td>PHIG2 (^{(b)})</td>
<td>V</td>
<td>(EASUB + BG0SUB) for n-well; (EASUB) for p-well</td>
<td>-</td>
<td>-</td>
<td>well or back gate workfunction, eV, it will be modified according to NBG later in the code if 1) the back gate is NOT metallic and 2) its value is not provided by user</td>
</tr>
<tr>
<td>EPSRSUB</td>
<td></td>
<td>11.9</td>
<td>-</td>
<td>-</td>
<td>Relative dielectric constant of the substrate material</td>
</tr>
<tr>
<td>EPSROX1</td>
<td></td>
<td>3.9</td>
<td>-</td>
<td>-</td>
<td>Relative dielectric constant of the front gate insulator material</td>
</tr>
<tr>
<td>NSD(^{(b)})</td>
<td>(m^{-3})</td>
<td>2e26</td>
<td>2e25</td>
<td>1e27</td>
<td>S/D doping concentration</td>
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</table>
### 6.4 Basic Model Parameters

Note: binnable parameters are marked as: (b)

<table>
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<tr>
<th>Name</th>
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<th>Default</th>
<th>Min</th>
<th>Max</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>CIT (b)</td>
<td>F/m²</td>
<td>0.0</td>
<td>-</td>
<td>-</td>
<td>Parameter for interface trap</td>
</tr>
<tr>
<td>CDSC (b)</td>
<td>F/m²</td>
<td>0.14</td>
<td>0.0</td>
<td>-</td>
<td>Coupling capacitance between S/D and channel</td>
</tr>
<tr>
<td>CDSCD (b)</td>
<td>F/m²V</td>
<td>0.14</td>
<td>0.0</td>
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<td>Drain-bias sensitivity of CDSC</td>
</tr>
<tr>
<td>CBGCBG (b)</td>
<td>F/m²V</td>
<td>0.1</td>
<td>0.0</td>
<td>-</td>
<td>Back-gate bias sensitivity of coupling capacitance to channel</td>
</tr>
<tr>
<td>CBGCBG0 (b)</td>
<td>F/m²V</td>
<td>0.0</td>
<td>0.0</td>
<td>-</td>
<td>Backgate-Bias sensitivity of SS for long channel</td>
</tr>
<tr>
<td>CBGCBGP (b)</td>
<td>F/m²V²</td>
<td>0.0</td>
<td>0.0</td>
<td>-</td>
<td>Sublinear Backgate-Bias sensitivity of SS for long channel</td>
</tr>
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<td>CBGCBGD (b)</td>
<td>F/m²V²</td>
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<td>0.0</td>
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<td>Nonlinear backgate-bias sensitivity of SS</td>
</tr>
<tr>
<td>DVT0 (b)</td>
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<td>SCE coefficient</td>
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<td>DVT1 (b)</td>
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<td>-</td>
<td>SCE exponent coefficient</td>
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<td>PHIN (b)</td>
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<td>Nonuniform vertical doping effect on surface potential</td>
</tr>
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<td>ETA0 (b)</td>
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<td>DIBL coefficient</td>
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<tr>
<td>ETAB (b)</td>
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<td>DIBL coefficient-Back Gate Bais Dependence</td>
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<td>DIBL exponent coefficient</td>
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<tr>
<td>K1RSCE (b)</td>
<td>V¹/²</td>
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<td>-</td>
<td>-</td>
<td>Prefactor for reverse short channel effect</td>
</tr>
<tr>
<td>LPE0 (b)</td>
<td>m</td>
<td>8.2e-9</td>
<td>-Leff</td>
<td>-</td>
<td>Equivalent length of pocket region at zero bias</td>
</tr>
<tr>
<td>DSC0</td>
<td>m</td>
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<td>-</td>
<td>-</td>
<td>Parameter for short channel effect at moderate L and high drain bias</td>
</tr>
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<td>DSC1</td>
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<td>Parameter for short channel effect at moderate L and high drain bias</td>
</tr>
<tr>
<td>ASCL</td>
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<td>Parameter for back-gate dependent scale length</td>
</tr>
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<td>Parameter for back-gate dependent scale length</td>
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<tr>
<td>VSAT (b)</td>
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<td>Saturation velocity in the saturation region</td>
</tr>
<tr>
<td>Name</td>
<td>Unit</td>
<td>Default</td>
<td>Min</td>
<td>Max</td>
<td>Description</td>
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<td>------</td>
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<tr>
<td>AVSAT(^{(b)})</td>
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<td>-</td>
<td>-</td>
<td>Saturation velocity in the saturation region for short channel devices</td>
</tr>
<tr>
<td>BVSAT(^{(b)})</td>
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<td>100.0e-9</td>
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<td>Saturation velocity coefficient in the saturation region for short channel devices</td>
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<tr>
<td>VSATB(^{(b)})</td>
<td>1/V</td>
<td>0.00</td>
<td>0.0</td>
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<td>Saturation velocity parameter for Back Gate Bias dependence on mobility at high Vds</td>
</tr>
<tr>
<td>AVSATB(^{(b)})</td>
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<td>0.0</td>
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<td>Saturation velocity parameter for Back Gate Bias dependence on mobility at high Vds for short channel devices</td>
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<td>0.0</td>
<td>-</td>
<td>Saturation velocity parameter for Back Gate Bias dependence on mobility at high Vds for short channel devices</td>
</tr>
<tr>
<td>VSAT1(^{(b)})</td>
<td>m/s</td>
<td>VSAT</td>
<td>-</td>
<td>-</td>
<td>Saturation velocity in the linear region</td>
</tr>
<tr>
<td>AVSAT1(^{(b)})</td>
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<td>AVSAT</td>
<td>-</td>
<td>-</td>
<td>Saturation velocity in the linear region for short channel devices</td>
</tr>
<tr>
<td>BVSAT1(^{(b)})</td>
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<td>BVSAT</td>
<td>-</td>
<td>-</td>
<td>Saturation velocity coefficient in the linear region for short channel devices</td>
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<tr>
<td>VSATCV(^{(b)})</td>
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<td>VSAT</td>
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<td>Saturation velocity for the saturation region for C-V</td>
</tr>
<tr>
<td>AVSATCV(^{(b)})</td>
<td>m/s</td>
<td>AVSAT</td>
<td>-</td>
<td>-</td>
<td>Saturation velocity in the saturation region for short channel C-V</td>
</tr>
<tr>
<td>BVSATCV(^{(b)})</td>
<td>m/s</td>
<td>BVSAT</td>
<td>-</td>
<td>-</td>
<td>Saturation velocity coefficient in the saturation region for short channel C-V</td>
</tr>
<tr>
<td>DELTA SAT</td>
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<td>Velocity saturation parameter</td>
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<td>KSUBIV(^{(b)})</td>
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<td>-</td>
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<td>MEXP(^{(b)})</td>
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<td>AMEXP(^{(b)})</td>
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<td>PTWG(^{(b)})</td>
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<td>APTWG(^{(b)})</td>
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<td>-</td>
<td>-</td>
<td>Correction factor for velocity saturation in short channel devices</td>
</tr>
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### 6.5 Parameters for Temperature Dependence and Self Heating

Note: binnable parameters are marked as: \((b)\)

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References


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- Hancheng Liang (Proplus Solutions)
- Sally Liu (TSMC)
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- Joddy Wang (Synopsys)
- Qingxue Wang (Synopsys)
- Josef Watts (IBM)
- Richard Williams (IBM)
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